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Electronics

THE WORLDWIDE TECHNOLOGY WEEKLY

JULY 15, 1985

CAN U.S. CHIP MAKERS MAKE IT IN JAPAN?

PAGE 30

CHIPS FINALLY ARRIVE FOR IBM TOKEN-RING NETWORK/16

A RISC COMPUTER THAT LIKES FLOATING POINT/48

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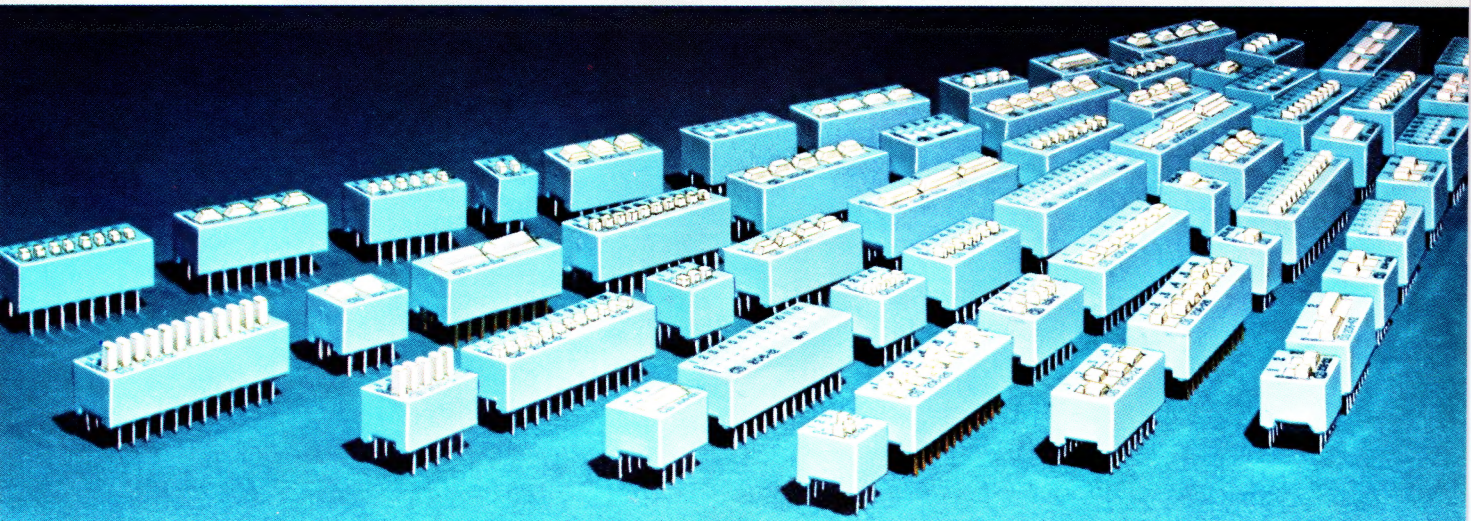

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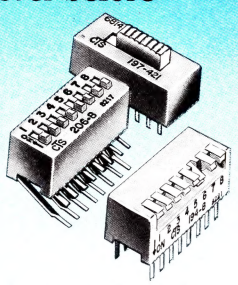

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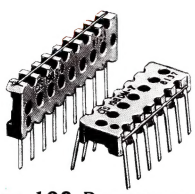

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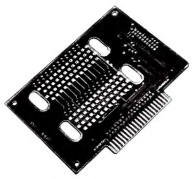

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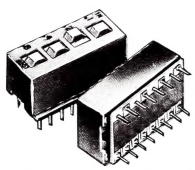

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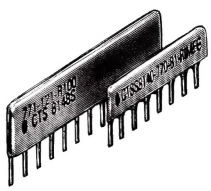

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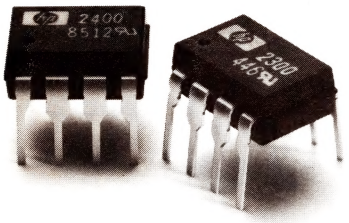

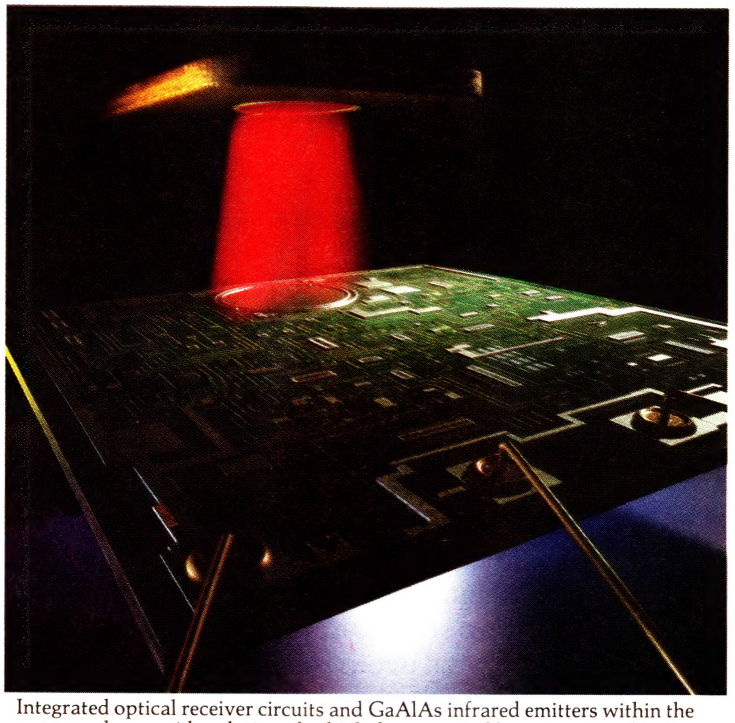

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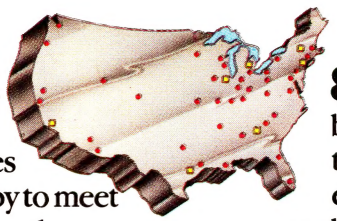

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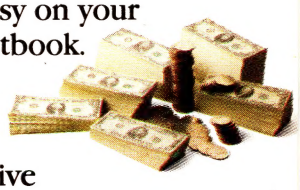

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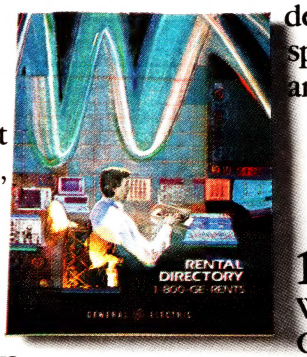

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JULY 15, 1985 VOLUME 58, NO. 28

Electronics

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Cover design: art director Fred Sklenar. Photo: Joe Ruskin

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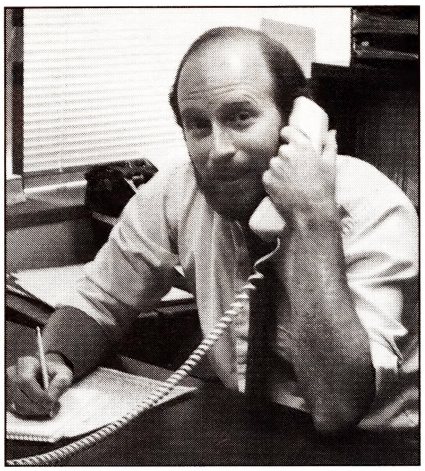
Veteran journalists know that for every big story that breaks with an explosion, there are dozens of others that surface slowly and simmer quietly for years. One such story is "TI's chips ready for IBM token-ring LAN," on p. 16. It was written in Dallas by J. Robert Lineback, with help from Clifford Barney in Palo Alto.

Rob recalls that he first heard about IBM Corp.'s early interest in working with Texas Instruments Inc. on what later turned out to be the five-chip token-passing ring adapter three years ago. That was at the 1982 National Computer Conference, in Houston. "And this week, the 1985 edition of the conference is taking place in Chicago with the token-ring introduction still delayed—but now it's certain to come in the second half," predicts Rob.

Since the formal announcement of the joint development project in September 1982, he says, IBM and TI have dropped only scattered hints about the token-ring adapter and the local-area network. But he has little doubt that the token-ring pot will heat to a boil this summer as IBM makes its move.

One clue is that often-asked questions about the status of the five-chip set are no longer getting "no comment" replies. Though most of the queries are the same, the responses are changing—making new insight into the LAN strategy possible.

"Also," Rob adds, "information is starting to seep from early beta-test sites that have working samples of the token-ring chips from TI under nondisclosure agreements. Potential token-ring network vendors, such as Ungermann-Bass Inc., of Santa Clara, Calif., are now starting to talk about products that are waiting in the wings for the IBM announcement."



Following up. Lineback at work in Dallas.

In Cliff Barney's view, "The interesting part of the token-ring story was that it was a cooperative effort. I had been told about the Ungermann-Bass chip set and asked Rob to see what was happening at TI, where he found out about the IBM protocol superset. We decided we had a pretty good story, with a lot of new information. Rob organized and wrote it, and I checked with the IEEE-802.5 ring committee to see what was happening on that front"—it met last week in Vancouver. Cliff says that he particularly enjoys doing this kind of cooperative piece: "It gives good added value to the bureau system."

Laurence Altman

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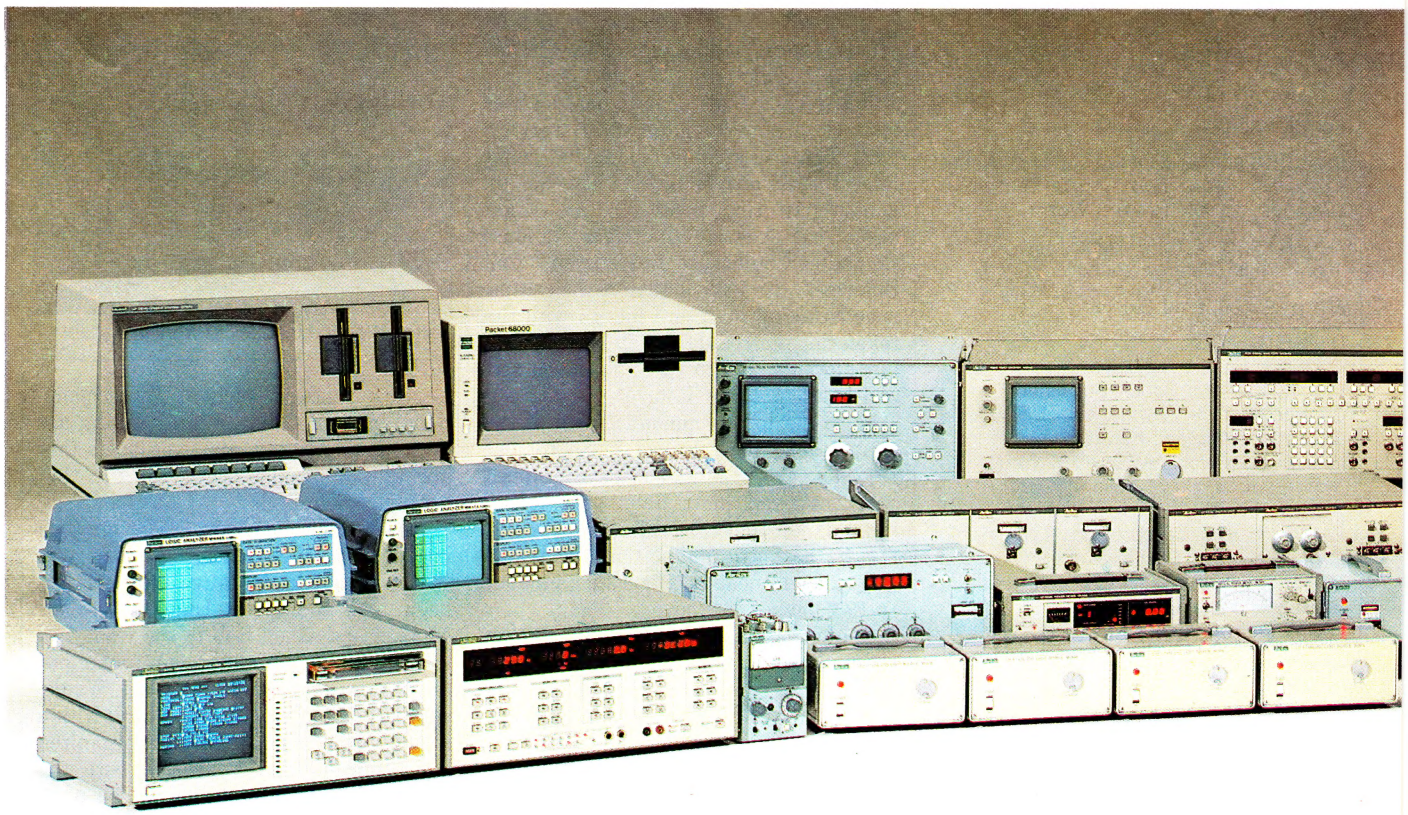

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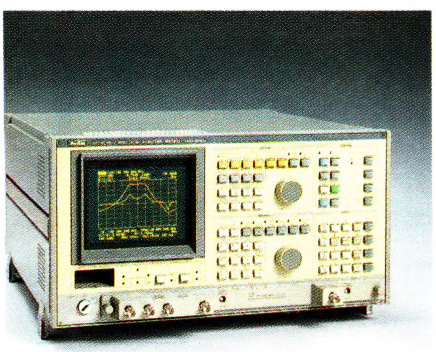

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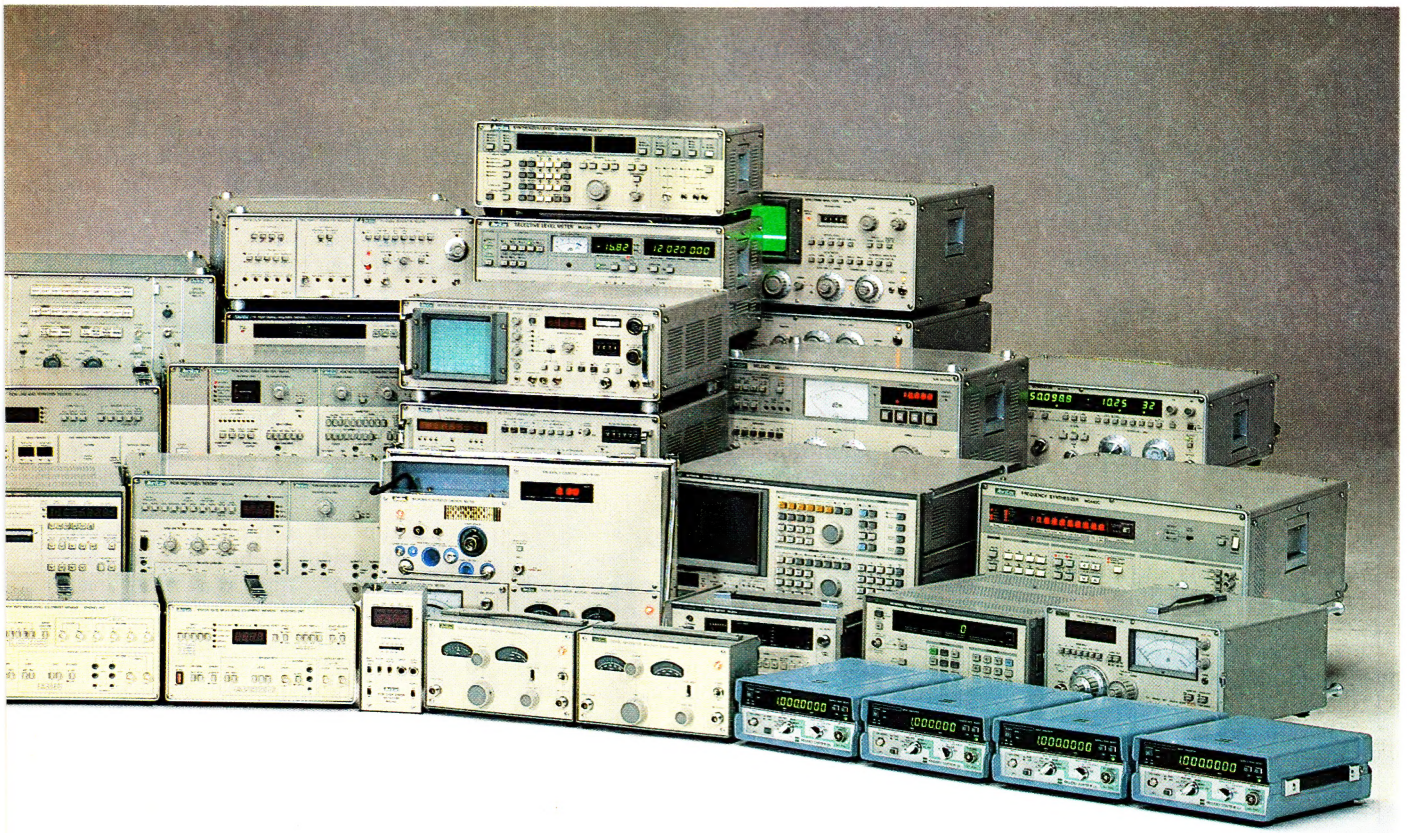

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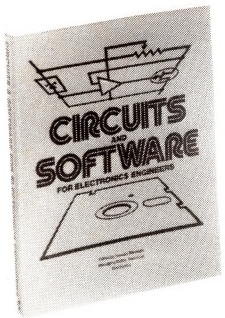

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MEETINGS

IJCAL-85, International Joint Conferences on Artificial Intelligence Inc. *et al.* (Steve Crocker, Aerospace Corp., P.O. Box 92957, Los Angeles, Calif. 90009), University of California, Los Angeles, Aug. 18-24.

Intech '85—Integrated Information Technology Conference and Exposition, National Trade Productions Inc. (2111 Eisenhower Ave., Alexandria, Va. 22314), Moscone Center, San Francisco, Aug. 26-30.

International Conference on Magnetism, International Union of Pure and Applied Physics *et al.* (Diane Suiters, Courtesy Associates, 655 15th St., N.W., Washington, D.C. 20005), Hilton Hotel, San Francisco, Aug. 26-30.

Seventh Quartz Devices Conference and Exhibition, Electronic Industries Association (2001 Eye St., N.W., Washington, D.C. 20006), Westin Crown Center, Kansas City, Mo., Aug. 27-29.

Advanced Manufacturing Techniques in Electronics, Institution of Electronic and Radio Engineers (99 Gower St., London WC1E 6AZ, UK), University of Edinburgh, Edinburgh, Scotland, Sept. 2-4.

Orcal '85—Orange County Manufacturing and Metalworking Conference and Exposition, Society of Manufacturing Engineers and American Society for Metals (SME, 1 SME Dr., Dearborn, Mich. 48121), Convention Center, Anaheim, Calif., Sept. 4-6.

Third Videotex Congress, Swiss Industries Fair (Congress Secretariat of the Swiss Industries Fair, Messeplatz 22, 4021 Basel, Switzerland), World Trade and Convention Center, Basel, Sept. 5-6.

Byte Computer Shows, The Interface Group Inc. and *Byte* magazine (The Interface Group, 300 First Ave., Needham, Mass. 02194), Convention Center, Dallas, Sept. 5-7; New York Coliseum, New York, Sept. 19-21; Brooks Hall, San Francisco, Sept. 26-29.

OEM Design '85 Show and Conference, Penton Exposition Division (Howard Freed, Exhibits Manager, Penton Exposition Division, 1111 Chester Ave., Cleveland, Ohio, 44114), Civic Center, Philadelphia, Sept. 9-11.

Federal Computer Conference, National Council for Education on Information Strategies (M. Sullivan-Trainor, Federal Computer Conference, P.O. Box N, Wayland, Mass. 01778), Convention Center, Washington, Sept 9-11.

Compint '85—Computer Aided Technologies Conference, IEEE (Stephen G. Leahey, P.O. Box 577, Desjardins Postal Station, Montreal, Quebec, Canada H5B 1B7) Palais des Congres, Montreal, Sept. 9-12.

15th European Microwave Conference, Société Française des Electriciens, (Microwave Exhibition & Publishers Ltd., Convex House, 43 Dudley Rd., Tunbridge Wells, Kent, TN1 1LE, UK), Palais des Congres, Paris, Sept. 9-12.

SEMINARS

Artificial Intelligence and Software Engineering, Data Processing Management Association (Technology Training Corp., P.O. Box 3608, Torrance, Calif. 90510), Park Plaza, Boston, Aug. 26-27.

Workshop on Coupling Symbolic and Numerical Computing in Expert Systems, American Association for Artificial Intelligence (Janusz A. Kowalik, Boeing Computer Services, M/S 7A-03, P.O. Box 24346, Seattle, Wash. 98124), Boeing Computer Services AI Center, Bellevue, Wash., Aug. 27-29.

Surface-Mount Technology Seminar, Worldwide Convention Management Co. (17730 W. Peterson Rd., Libertyville, Ill. 60048-9989), Summit Hotel, Dallas, Sept. 10-11; Hyatt Regency Woodfield, Chicago, Oct. 17-18; Sheraton, Boston, Nov. 19-20; LeBaron Hotel, San Jose, Calif., Dec. 5-6.

Silicon Processing for the VLSI Era, University of California Extension (P.O. Box AZ, Irvine, Calif. 92716), Pembroke College, Cambridge University, London, Sept. 9-13.

Personal Computer Industry: Opportunities and Pitfalls, Future Computing Inc. (8111 LBJ Freeway, Dallas, Texas 75251), Westin Hotel, Dallas, Sept. 10-11.

VHSIC Applications Workshop, Department of Defense (Palisades Institute for Research Services, Inc., 201 Varick St., New York, N.Y., 10014), David Sarnoff Research Center, Princeton, N.J., Sept. 10-12.

Teleconferencing—Technology, Applications, Equipment, and Effective Utilization, Frost & Sullivan Inc. (Carol Every, Frost & Sullivan, 106 Fulton St., New York, N.Y. 10038), Selfridge Hotel, London, Sept. 10-13.

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FUNCTION	USE	TECHNOLOGY	
		BIPOLAR	BIFET/CMOS
OPERATIONAL AMPLIFIERS	General purpose	UA 709-UA 741	**BIFET** LM 351-LM 353 TL 081-TL 082 TL 084
	Precision	LM 101-LM 101 A LM 11	
	Low noise	LM 108-LM 108 A	TL 071-TL 072 TL 074
	Low consumption	LM 124	TL 061-TL 062 TL 064
	Single voltage	LM 158-LM 134	
	Low bias current		LF 155-LF 156 LF 157
VOLTAGE REGULATORS	Fixed negative output	UA 79XX series	
	Fixed positive output	LM 123 UA 78XX series	
	Adjustable negative output	LM 137	
	Adjustable positive output	LM 105-LM 117 LM 138	
VIDEO CONVERTERS	6 bits-Flash A/D 8 bits-Flash A/D 8 bits-D/A		**CMOS** TS 8306 TS 8308 TS 8408
F/V AND V/F CONVERTERS	A/D high speed 4 bits Voltage-Frequency	UAC 1005 LM 131	
SAMPLE AND HOLD	Precision: 12 bits		**BIFET** LF 198
ACTIVE FILTERS	Low pass, high pass and band pass. Butterworth, Cauer Tchebychef. 3 to 8 poles		**CMOS** TS 85XX series
TIMERS	High stability Adjustable	SE 555 SE 556	

● MICROPROCESSORS AND PERIPHERALS

PRODUCT REFERENCE	Speed MHz	− 40, + 85 °C		− 55, + 125 °C				MIL STD 883			
		Cerdip	Ceramic	Cerdip	Ceramic	LCC	PGA	Cerdip	Ceramic	LCC	PGA
6800 family (1)	1	●	●	●	●	●		●	●	●	
68A00 family (2)	1.5	●	●								
TS 68HC05E2	4	●	●		●						
TS 68000	8		●		●	●	●		●	●	●
TS 68000	10		●		●	●	●		●	●	●
TS 68000	12		●		●	●	●		●	●	●
TS 68008	8		●		●				●		
TS 68008	10		●		●				●		
TS 68230	8		●		●	●			●	●	
TS 68230	10		●		●	●			●	●	
2900 family (3)					●	●	●		●	●	●
TS 4442					●				●		
TS 29747					●				●		

(1) includes the TS 6800, 6802, 6803, 6803-1, 6809, 6809-E, 6810, 6821, 6840, 6850, 6852, 6854.
(2) includes the TS 68A00, 68A02, 68A09, 68A10, 68A21, 68A40, 68A50, 68A52, 68A54.
(3) includes the TS 2901B, 2901C, 2902A, 2909A, 2910, 2911A, 2914, 2915A, 2917A, 2918, 2919.

● MEMORIES

PRODUCT REFERENCE		Access time (ns)	CASE				MIL STD 883
			Cerdip	Ceramic	LCC	Slim Line	
Bipolar PROM							
TS 71191	2 K x 8	80	●	●	●		●
TS 71191 A	2 K x 8	60	●	●	●		●
TS 71191 B	2 K x 8	45	●	●	●		●
TS 71191 C	2 K x 8	35	●	●	●	●	●
C.MOS EPROM							
TS 27 C 16	2 K x 8	450	●				●
TS 27 C 32	4 K x 8	450	●				●

● GATE ARRAYS

PRODUCT REFERENCE	Number of elements	Maximum frequency (MHz)
Bipolar Analog		
EFZA	425	500
EFZG	839	500
Bipolar Digital (ECL)		
EFZL	1200	200
EFZM	1700	200
HCMOS Technology		
EFGG	300	35
EFGH	650	35
EFGJ	1000	35
EFGK	1500	35
High Speed HCMOS Technology 2 metal layers		
EFGL	1400	50
EFGM	2000	50

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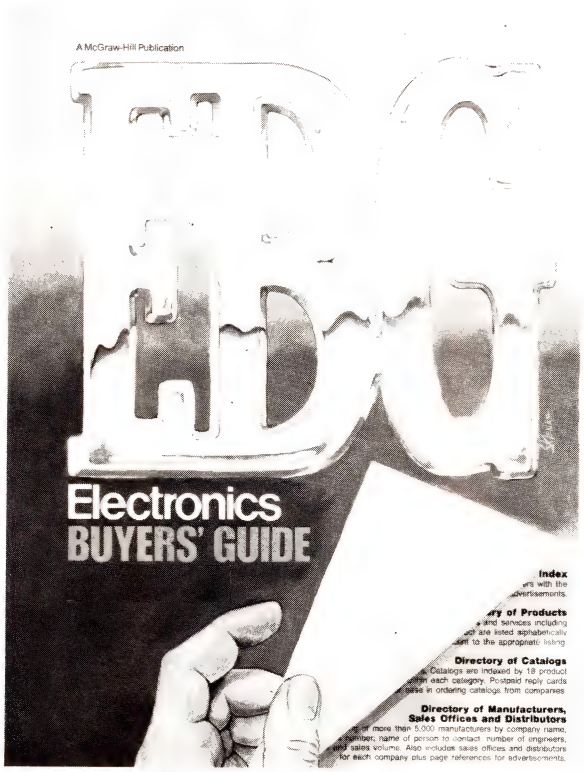

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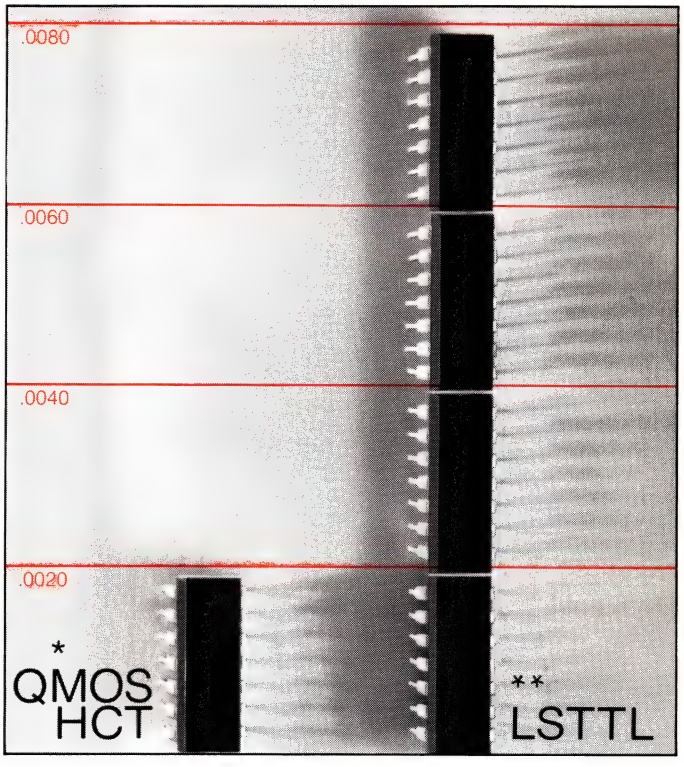
Rate of failure

(in % per 1,000 hours of testing at 60% confidence level, at 85° C).



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ELECTRONICS NEWSLETTER

JAPAN CHIP BUSINESS COULD FALL 10% TO 15% THIS YEAR

Japan's semiconductor industry this year will see its business drop 5% to 10%, and perhaps even 15%—the industry's first decline in 10 years, according to a report by the leading Japanese financial daily, *Nihon Keizai Shimbun*. The newspaper says that the main cause of the rapidly bulging warehouses and precipitous drop in prices is the poor sales of personal computers in the U.S. A slightly more optimistic outlook comes from Dataquest Japan Ltd., which predicts that production will range from flat to up 3% or 4%. Among the worst-hit companies are Hitachi, Fujitsu, and Oki Electric, whose production of memory circuits is relatively high. A Hitachi spokesman says that "reflecting current circumstances, a 10% decline in semiconductor production and a 20% decline in capital spending for semiconductors are not improbable." Japanese semiconductor production rose at a compound rate of 28% for the past nine years. Last year alone, it increased by more than 66%, to reach $10.6 billion. About half Japan's semiconductors are said to be exported directly or indirectly (in products) to the U.S. □

NEW JAPANESE OPEN-MARKET STANDARDS DISAPPOINT U.S.

The Japanese government gave some indication last week of how it plans to reform a wide variety of market-entry standards and product certifications, but the news disappointed U.S. electronics industry and government people in Tokyo. "The package doesn't include any of the key items in our trade negotiations with the Japanese," said a U.S. Embassy official. "And if it goes through the Diet in the fall as is, which seems likely, there is the danger of another backlash in Washington." John P. Stern, senior representative of the American Electronics Association's Tokyo office, found three major flaws in the Japanese announcement. "Prime Minister [Yasuhiro] Nakasone has been calling officials on the carpet in an effort to get action," he says, "but the bureaucracy clearly hasn't yet been sold on this program. There also has not been adequate consultation on the issue with the foreign business community, and there is no long-term commitment to reform, since the procedures would be reviewed after three years."

Moving toward its own open-market policy, Nippon Telegraph & Telephone Corp. last week decided to discontinue its practice of setting purchase targets for foreign products. Ichio Kata, chief of international procurement for NTT, says the company is "still looking for the best product at the best price," but strictly on an open-market basis. NTT procurement of foreign products rose from $16.1 million in 1980, when it first accepted open bids, to $143 million last year, when foreign products—mostly U.S.—accounted for about 6% of its telecommunications product purchases. □

NEW COMPETITION COMING FOR NETWORK SYSTEMS

Network Systems Corp., the Minneapolis outfit that dominates the market for high-speed, mixed-vendor, mainframe-to-mainframe networking systems, is about to face a challenge from Computer Network Technology Corp. The two-year-old New Hope, Minn., company, whose founders include former Network Systems employees, expects to wrap up beta tests at McDonnell Douglas Corp. this month on its Lanlord high-speed networking system. It plans to ship the first units next month. Computer Network Technology claims that using multiple 68000s and 2901 bit-slice processors coupled with up to 10 megabytes of memory per unit will give it an edge: its adapters for connecting mainframes to its net will allow Lanlord, running at 25 Mb/s, to equal or improve the message throughput of Network System's Hyperchannel, the de facto industry standard. What's more, at about $25,000 per adapter, the net sells for about half Hyperchannel's cost per node. □

ELECTRONICS NEWSLETTER

NEW RISC PROCESSORS FROM PYRAMID BOOST PRICE-PERFORMANCE

Pyramid Technology Corp., a pioneer in reduced-instruction-set computers, will boost state-of-the-art RISC performance by introducing at this week's National Computer Conference in Chicago a new high-end system based on a balanced pair of RISC processors. The Pyramid 90x series of Unix systems will improve the price-performance ratio with this dual-processor version of its multiuser Unix RISC systems, the company says. The Pyramid systems are built with register-intensive RISC processors running a version of Unix, called OSx, incorporating both popular Unix versions—Berkeley 4.2 and AT&T Co.'s System V. This architecture may open the door to future multiprocessor RISCs that will deliver very high-performance at much lower costs than, for example, a VAX 8600 [see related story, p. 54]. □

PRIAM DECIDES AT LAST MINUTE TO SHOW NEW DRIVES AT NCC

Introducing its first products since its merger with Vertex Peripherals Corp., Priam Corp. decided at the last minute to bring its new line of 5¼-in. hard-disk drives to the National Computer Conference. The San Jose, Calif., maker is introducing its model 514 (with 140-megabyte capacity on six platters) and 519 (with 191 megabytes on eight platters). Both products feature 20-ms average access time and an ST 412/506 interface. Evaluation quantities should be available late in the third quarter of this year, with volume shipments by year's end. The price for original-equipment manufacturers is $1,750 for the model 514 and $1,910 for the 519. □

OPTICAL-MEMORY CONTROLLER FOR IBM PC TO BOW AT NCC

Personal computer users dreaming of optical memories will get a glimmer of light at this week's NCC when Optotech Inc., the Colorado Springs maker of write-once optical drives, shows a controller for IBM Corp. Personal Computers. The controller, however, is more a tool than a product. It requires changes in applications software, so applications developers will likely be the first to use it. Optotech is shipping the controller with original-equipment-manufacturer evaluation units of its 400-megabyte 5984 write-once, read-mostly drive. A mass-market version will follow. □

WESTERN DIGITAL SHRINKS 3½-IN. DRIVE CONTROLLER TO ONE BOARD

Through surface-mounting techniques and new proprietary custom chips, Western Digital Corp., Irvine, Calif., has shrunk drive and controller circuitry for 20-megabyte 3½-in. disk drives onto one board. With samples available by the fall, the product's significance lies in its potential of cutting total price of the hard disks by up to 50% by the end of 1986, making them competitive with floppy disks, the company says. The board eliminates more than 30 chips now needed for the control and drive tasks, with new devices integrating host interfaces, servo functions, and read/write channel circuitry. □

10-kb/s MODEM QUICKENS PC-TO-MAINFRAME COMMUNICATIONS

Companies eager to pare the costs of dial-up connections between personal computers and mainframes can look at Irma Fastlink, a 10-kb/s packetizing modem from joint-venture partners Digital Communications Associates and Telebit Data Systems. Using a technique called adaptive quadrature amplitude modulation, the modem's 68000 microprocessor sweeps from 300 to 3,600 Hz on a voice-grade channel in 8-Hz steps, dynamically calculating the signal-to-noise ratio with a TMS 320 digital-signal processor and adjusting the bit rate for each fixed-length packet according to line quality. □

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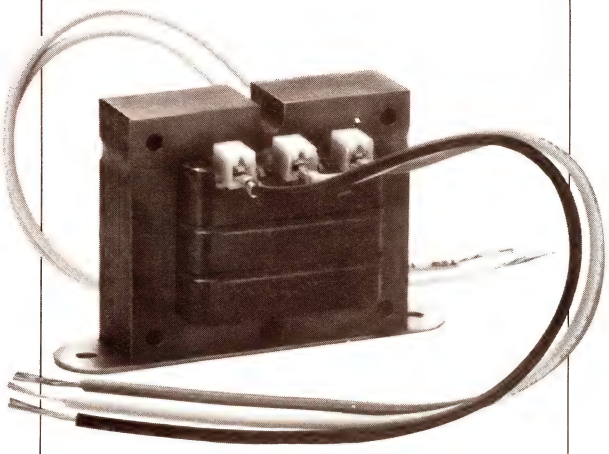

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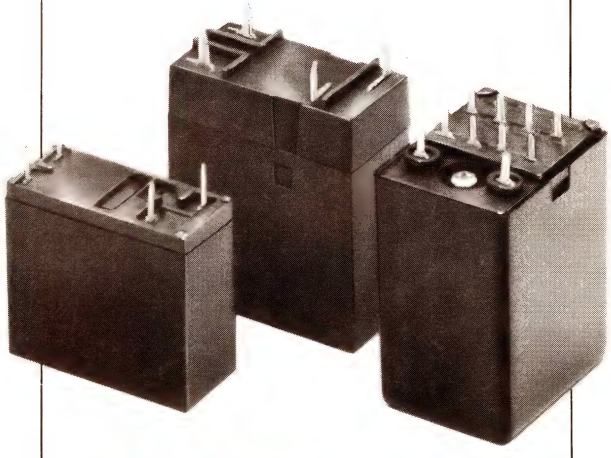


UNITED TECHNOLOGIES
HAMILTON STANDARD CONTROLS

Circle 75 on reader service card

THIS Electronics WEEK

THURSDAY *July 4*

While fireworks burst in celebration of the U.S.'s 209th birthday, sere winds continued to blow through the electronics industry. Silicon Valley and other industry centers looked like ghost towns as such companies as Advanced Micro Devices, Hewlett-Packard, Texas Instruments, and Wang Laboratories shut down for the entire week. Said Michael Kubiak, manager of statistical programs at the Semiconductor Industry Association: **"The vast majority of the layoffs have already occurred."** But he added that "everything is contingent on the fourth quarter." If business doesn't pick up, "more layoffs, four-day workweeks, and plant closings could be a possibility."

FRIDAY *July 5*

Digital Equipment Corp. filed suit against Emulex Corp. for patent infringements, seeking an injunction against the manufacture, marketing, and distribution of products that use its patented MSCP port protocol. The second-largest U.S. computer maker today asked the U.S. District Court in New Hampshire to prohibit Emulex, Costa Mesa, Calif., from making and selling its line of disk controllers, which are compatible with DEC's VAX, Microvax, and PDP-11 computers. Emulex is withholding comment until it reviews the suit.

MONDAY *July 8*

Raytheon Co. said it won **$77.2 million in U.S. Air Force contracts to produce specialized test equipment for the advanced medium-range air-to-air missile** (Amraam) program. The Massachusetts company is the second source for the beleaguered system, under development at Hughes Aircraft Co. . . . **Signetics Corp. announced a zero-defect warranty on all its semiconductor parts beginning Aug. 4.** The company said it is "incredibly obvious" that the entire electronics-components industry will eventually have to offer the same warranty—customers who find a defect in a lot can return the entire lot for factory rescreening.

TUESDAY *July 9*

United Technologies Corp. said it suspended construction on a $26 million expansion of its microelectronics research facility in East Hartford, Conn. The company, which owns Mostek Corp., the struggling chip maker, said it is reassessing its investment in the depressed semiconductor business. . . . Continuing its push into the electronics arena, **Eastman Kodak Co. said it would enter the fiber-optics market.** Its newly formed Lamdek Fiber Optics Division will market a high-precision connector for single-mode fiber near the end of this year.

WEDNESDAY *July 10*

Indesys Inc. (for Information Delivery System), a joint venture between Epson America and the ABC Video Enterprises unit of American Broadcasting Companies Inc., **will use the inaudible FM sideband of five ABC radio affiliates to transmit "any data that can be digitized,"** says Indesys president Michael Moone. Owners of IBM Corp. Personal Computers or compatibles will be able to use Indesys beginning in October through a $250 Epson erasable programmable read-only-memory receiver card that plugs into the PC's chassis. Customers without a PC can purchase a decoder box for about $300. Data flows at 38,400 baud, or about 1.5 pages per second. Initial markets will include New York, Los Angeles, San Francisco, Chicago, and Dallas, but plans call for eventual nationwide coverage. □

Electronics

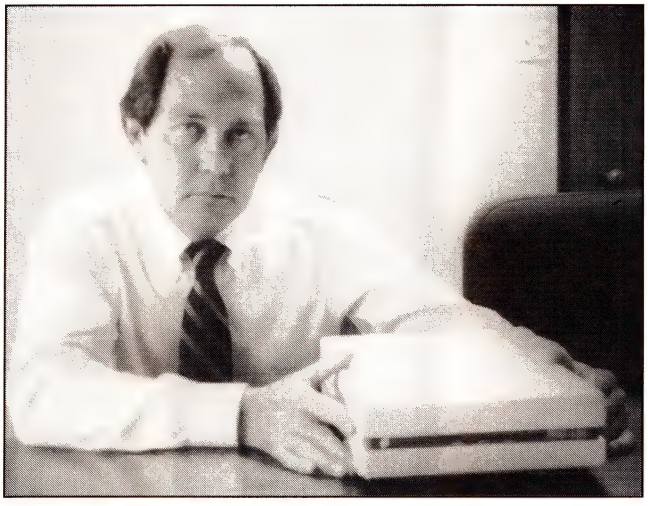
TI ANTES UP ITS CHIPS FOR IBM TOKEN-RING LAN

Overdue 4-Mb/s net's management functions embellish on 802.5 standard

Houston

After three years of hints, promises, and delays, it looks like IBM Corp. will introduce its 4-Mb/s token-ring local-area network within the next few months—perhaps as early as September. Texas Instruments Inc., the developer of the complex five-chip set upon which the IBM product is based, is supplying prototype chips to a number of computer-equipment vendors.

TI's Houston MOS operation is providing product-development support to many potential high-volume customers, and TI is reportedly making available tools for developing protocol software for the integrated circuits to some of its customers. The company has already wired several of its major plant and office sites to accept the LAN.



Holding fire. Ungermann-Bass has cards ready to use TI chips and IBM protocols, says Jim Jordan, its chief operating officer.

The long delay in introducing the network, in part due to difficulties with the complex chip set and in part to IBM's internal policies, gave other manufacturers the chance to prepare rival token-ring products. At least one, Ungermann-Bass Inc., Santa Clara, Calif., awaits only the IBM announcement to start marketing its own board-level line.

But potential competitors may have a problem. IBM has added a superset of proprietary LAN-management and diagnostic functions to the basic Institute of Electrical and Electronics Engineers 802.5 token-ring specification. Superset firmware is loaded into 16-K bytes of read-only memory on the protocol handler of a five-chip LAN adapter.

Eyes on IBM. IBM is also expected eventually to merge the token-passing network with protocols of its Systems Network Architecture, oriented to large computers. Despite slow progress, executives in the troubled computer industry are pinning hopes on IBM's long-awaited LAN. Office equipment vendors hope the token-ring will spark a strong LAN market and help revive stalled sales growth.

But the complexities of the extra services will make it extremely difficult to fully tap into IBM's network, say TI local-net-component managers. Equipment connectors must be based on the same adapter circuits as those being used by Big Blue.

Without exactly the same implementation of the services—such as error logging, reporting, and multiple-ring management—equipment attached to the network by other token-ring silicon adapters could be shut off from the working portion of the LAN whenever the system attempts to isolate hardware or software failures in real time.

"You cannot build in IBM compatibility strictly from the pages of the IEEE-802.5 spec," assures Richard Templeton, marketing manager for TI local-net components based in Houston. "There is simply not enough detail. Reliability of the ring is one of the traps some of our competitors will fall into."

Vendors hope IBM's ring will spark a strong LAN market

Reliability was one of the chief topics at last week's meeting of committee 802.5 in Vancouver, Canada. Token passing avoids circuit contention problems by allowing a station to transmit only when it possesses the token bit, which is passed from station to station. Ring reconfiguration when the token is lost is the Achilles' heel of the token-ring architecture, says committee chairman Robert Donnen.

"There are as many opinions about it as there are people who know about token rings," Donnen says. "And we are a long way from a solution."

Whether or not the IBM superset solves these problems in a proprietary way, Ungermann-Bass is ready with a complete line of board-level products. The company fully expects the boards to be compatible with the SNA-enhanced token-ring network from IBM.

Ungermann-Bass cards can be hooked to the network cable through standard logic parts or the two bipolar integrated media-interface circuits contained in TI's chip set, says Jim Jordan, chief operating officer of Ungermann-Bass. "We won't go into the chip business and sell against TI."

The company intends to use its gate-array 802.5-compatible chip set only in its own adapter-board line. The line includes a PC network interface unit (NIU) that plugs into the motherboard of the IBM personal computer; an NIU for terminals connected to the two RS-232-C ports of an IBM PC; an NIU with eight RS-232-C ports for attaching peripherals to the network; a Multibus NIU; a ring-to-ring bridge for hierarchical rings; and an active wiring center.

Factory first. Ungermann-Bass performed the token-ring work at its facility in Boca Raton, Fla., where researchers used some of the same chip technology to ready a two-chip token-bus net interface for the factory [*Electronics*, June 17, 1985, p. 19]. Completed before the factory-network chips, the office-oriented token-ring adapter boards are waiting in the wings. Other makers are also readying 802.5-compatible products

in anticipation of the IBM move; most are expected to add protocols to their products to fully participate in IBM's network.

"No one knows exactly what the IBM network will look like. It follows the [IEEE] specs, but the specs only go so far and there are so many options," says network consultant Harvey A. Freedman of Architecture Technology Inc., Minneapolis. In other network-technology markets, various protocols have emerged as vendors compete for market dominance. But in the token-ring arena, IBM should quickly set the pace.

"There are 100 or so vendors making Ethernet-type systems following the IEEE-802.3 spec now, and the degree of compatibility varies all over the board depending upon the chips they use and functions implemented," Freedman notes. "But in the token-passing area, anything that IBM announces will place pressure on you to conform if you want to continue selling products." He believes, however, that the complexity of a token-ring network will keep the price of IBM's LAN higher than simpler Ethernet-like links.

"How much lower [in price] is Ethernet going to go? From what I have seen of developments at manufacturers, the price of connection in the next year or so will be reduced to as low as $100," he adds, suggesting a pricing battle following the IBM announcement.

Cost point. But as the 1985 second-half introduction approaches, TI remains confident that the elaborate chip set will result initially in competitive net adapters priced at or below the $695 retail cost of IBM's slower broadband PC Network. Further, the power dissipation of the set's three largest chips is low enough for TI to plan to house the n-MOS processors in low-cost plastic. In the future, TI will apply processing technology from its 256-K random-access-memory fabrication lines to the 2.4-μm parts to further lower costs.

For months, TI has been testing the chips on a number of system-adapter boards, including a prototype for the IBM Personal Computer. TI's PC token-ring board is now being used as a marketing vehicle whenever net-chip managers visit prospective customers.

Complex services will make it hard to tap ring without TI chips

"The question that always comes up is, why five chips and why not three, or two like others are claiming?" admits Templeton, recounting recent calls to equipment makers. With the IBM-net-chip set, he points out, only a few passive resistors and capacitors are needed as glue parts around the two bipolar cable interface chips.

The PC Network board, he says, is a different story. Though based on a two-chip set from Sytek Inc., the board contains many discrete parts in its 2-Mb/s modem, plus large heat sinks and over 20 tuning pots.

Templeton says that TI opted to not use general-purpose microprocessors in its adapter implementation because both the chip maker and IBM feared system designers would inadvertently introduce incompatibility into the network through adapter-code development. Therefore, the basic LAN-management and testing services are fixed into the integrated adapter chip set. *–J. Robert Lineback and Clifford Barney*

LAN PROCESSORS READY FOR SPEED UPGRADE

The adapter chip set for IBM Corp.'s token-ring local-area network is intended to keep the LAN working in the office well into the next century. One such life-extending feature is the current chip set's high-speed capability. The three very-large scale integrated processors can handle data rates 10 times the current 4-Mb/s standard.

The IBM Corp. net-adapter architecture also contains a 3-MHz, 18-bit-wide bus connecting the system interface, communications, and protocol-handler processors. Texas Instruments Inc. uses n-MOS technology to make these three chips, so the net-adapter bus can pass data at 48 Mb/s. The speed comes partly from the bus's single-cycle contention-arbitration scheme. Using even very fast general-purpose microprocessors on the bus would have greatly slowed the adapter, taking three or four cycles to arbitrate, says Richard Templeton, marketing manager for network components.

The five-chip IBM network set is limited by two medium-scale bipolar MSI cable-interface chips to the 4-Mb/s data rate specified by the Institute of Electrical and Electronics Engineers' 802.5 protocol. The 802.5 committee has heard several proposals to increase the standard to 16 Mb/s—a move that chairman Robert Donnen says would require only a language change in the protocol because it poses no technical problems. The system-interface processor can handle up to 40 Mb/s. **–J. R. L.**

ARTIFICIAL INTELLIGENCE

AI BRINGS SMARTS TO PC-BOARD ASSEMBLY

El Segundo, Calif.

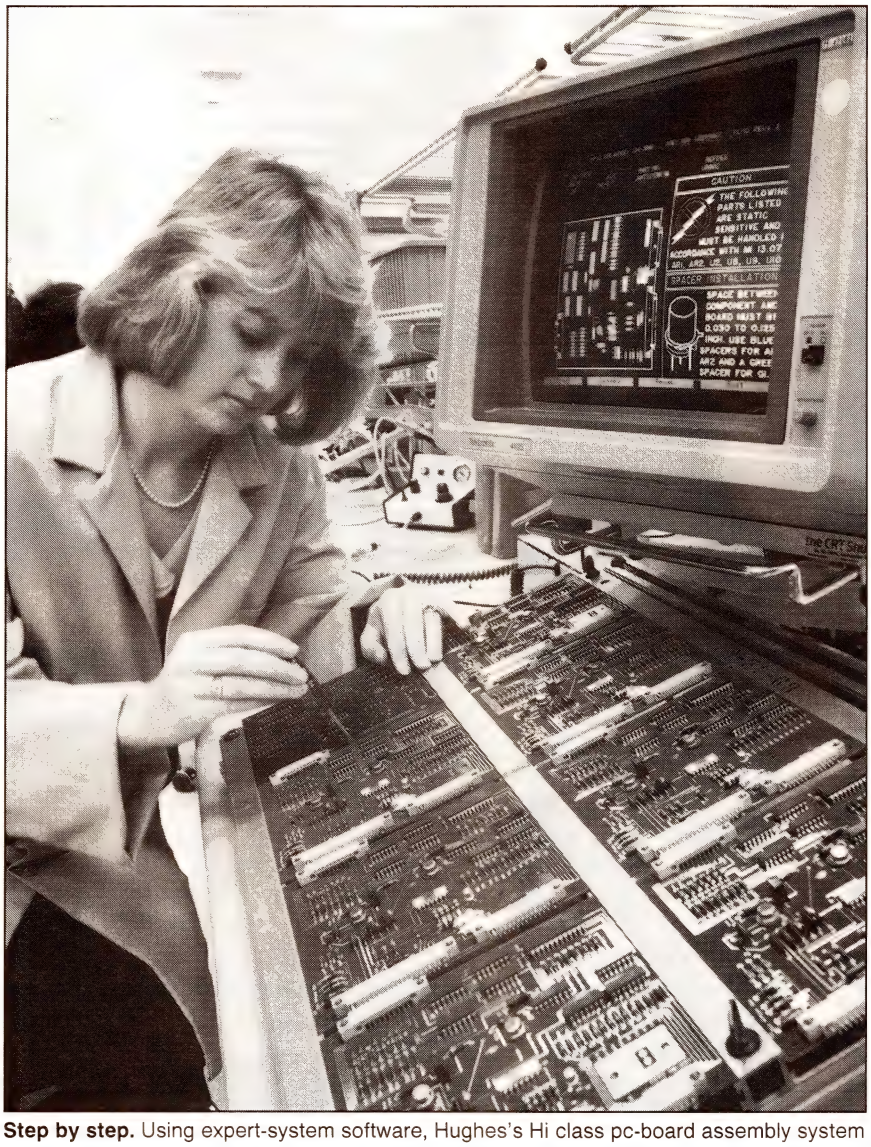
For all the hullabaloo that surrounds artificial intelligence, down-to-earth uses for the technique remain scarce. Virtually any application that makes the big jump from research into the real world will draw a crowd, as Hughes Aircraft Co. is discovering.

Word is out about the Hughes printed-circuit-board assembly system, whose software uses an expert system that sets up the sequence of hand-assembly steps. It also sorts design and specification information to be presented in step-by-step instructions to assembly workers [*Electronics*, July 8, 1985, p. 15]. The expert system also comes into play in bringing new information into the system for engineering changes and production-line tuning measures.

Hughes expects a significant payback from the expert system in reduced defect rates, but cannot yet quantify them. The system is also expected to slash paperwork costs, which it might have done without its inferential capabilities. The AI component is only part of a larger automated assembly system called the Producibility-based Automated Design and Manufacturing System. It is not yet linked to test equipment on the one hand or computer-aided-engineering systems on the other.

Installed last November, the Hi class (for Hughes Integrated Classification System) hardware consists of graphics terminals clustered around an Apollo work station. The worker's only input to the system during assembly is to press a foot treadle to advance to the next step; the system does not make inferences in real time in response to keyboard or other input. But the worker can suggest to the system operator a rule for the expert system or a warning to be displayed during some step.

Schematic rule base. From hundreds of hours of analyzing data from designers, planners, and assemblers in the pc-board production cycle, Hughes built a systematic rule base for the inference software that runs Hi class. "This is where the real effort lies," notes Joel A. Schnur, manager of com-



Step by step. Using expert-system software, Hughes's Hi class pc-board assembly system reduces the assembly process to a sequence of individual steps displayed on a video terminal.

puter-aided manufacturing. Hughes wrote all its own software.

Currently, the Electro-Optical and Data Systems Group at this Hughes facility uses Hi class to assemble two types of pc boards at five terminals. By the end of this year, Hughes hopes to be producing some 32 types of boards at 60 work stations.

An AI system that is already doing practical jobs is a milestone in a field marked by overoptimistic promises and a dearth of success stories, says Harvey P. Newquist III, editor of "AI Trends," a Scottsdale, Ariz., newsletter. "That's really a neat step, and something the industry is waiting for, actually working and saving bucks." Newquist says that he has heard of no other such system. Nor have Hughes officials, based on their own research and inquiries from other companies.

Yet Hughes had no intention of being a trailblazer, says Schnur. "Our goal is to make money by improving the quality of manufacturing, which is the real world." After attending AI meetings and perusing the literature, Schnur concluded that other AI researchers took more interest in "adding bells and whistles to lab prototypes."

Schnur credits the engineers who were recently recruited from top universities—"our young superstars"—for steering the project of streamlining pc-board manufacturing toward AI. "They talked us into it on a small scale and then we demonstrated it would work in a prototype," he says. Initial planning began in 1981; the pilot program that linked the software and hardware went into operation last year.

Though AI experts have assumed that the Lisp programming language will dominate most AI work, Hughes chose another route. Its researchers started with Fortran, switched to Pascal, and are now converting everything to the highly portable C language. Nor did the company use expert-system development tools.

Design changes. The Hughes system also eliminates paper—instruction manuals, specifications, tooling requirements, and the like. There is a related advantage: better control when there are many design changes. When changes take place on assembly operations run by Hi class, information goes directly into the data base, eliminating the delays and mistakes associated with such changes on paper.

This benefit is especially attractive to companies with defense programs, notes Sy Schoen, staff scientist at Litton Industries Inc., Beverly Hills, Calif. His responsibility for coordinating the company's AI activities puts him in close touch with such developments. "The best thing of all is this ability to respond to engineering changes."

Doing away with paper is also saving a lot of time, notes Schnur. Organizing all the documents and instructions for a program used to take about 140 hours. Now it takes only about 30 hours.

For now, the AI-based system is only for internal Hughes production, says Schnur, but outside inquiries are coming in fast. *–Larry Waller*

MILITARY

GAO RAPS PENTAGON ON VHSIC SPENDING

Washington

The fiscal watchdog of the U.S. Congress says the Defense Department may be spending money on the VHSIC program faster than it should.

In a report on the Pentagon's Very High-Speed Integrated Circuits program, issued without fanfare in May, the General Accounting Office criticized the DOD's decision to expand subsidies to stimulate earlier application of the technology when development, demonstration, and independent testing lag behind schedule. The GAO's 12-page assessment of the program estimates that the cost swelled from $339 million to at least $781 million—and perhaps more than $1 billion—when the DOD decided in 1982 to directly subsidize the six Phase 1 VHSIC contractors.

"There is evidence that the DOD and the VHSIC contractors have encountered significant delays and other problems in developing, demonstrating, and

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verifying the first-generation VHSIC technology," the report says. "Because of these problems, we have concerns about the DOD's emphasis on program expansion before the technology has been fully developed and tested."

The DOD started the VHSIC program in 1981 to develop and demonstrate advanced data- and signal-processing technology for defense systems. Though demonstration of Phase 1 prototypes was set for May 1984, several contractors still may not be ready until later this year—18 months behind schedule.

IBM Corp.'s Federal Systems Division was the only Phase 1 contractor to deliver its prototype on time last May. Since then, Honeywell Inc. has demonstrated its VHSIC chip set, while TRW Inc.'s Military Electronics Division has demonstrated two thirds of its chips.

The other three contractors—Hughes Aircraft, Texas Instruments, and Westinghouse Systems Development Division—expect to complete Phase 1 requirements this year, according to the office of the under secretary of defense for research and engineering.

GAO scores use of subsidies for early applications

The GAO report takes to task a $192 million yield-enhancement and manufacturing-technology subsidy to increase the quantity and cut the cost of VHSIC chips produced by contractors, and a $148 million technology-insertion subsidy (which the Pentagon wants to expand to $210 million) to increase system designers' demand for VHSIC chips in the near future (see chart).

The yield-enhancement subsidy's goals are to increase contractors' manufacturing yields to 10% from less than 2% while cutting the unit cost of VHSIC chips from $5,000 to about $500 by 1987. The GAO proposes that the DOD continue yield-enhancement subsidies depending on contractors' progress.

The report says the DOD has committed $148.2 million for 38 potential system applications and will provide an additional $62.2 million for more potential applications. But the GAO recommends the additional monies not be approved and that, instead, the DOD should complete Phase 1.

Though agreeing with the GAO's finding that the VHSIC program has now ballooned beyond its original aims, James P. Wade Jr., acting under secretary of defense for research and engineering, disagrees with other conclusions. In an 11-page DOD response published with the GAO report, Wade defends expanding the VHSIC program, arguing that it was "necessary to insure that the technology which was being developed and demonstrated in Phase 1 would be available and reasonably priced to enhance the chances of inserting the technology into military systems in a timely manner."

Wade also disagrees with the GAO's recommendation that the Pentagon not approve the $62.2 million set aside for more VHSIC insertion efforts. Because the Pentagon agrees with a GAO recommendation making continued yield-enhancement funding contingent upon contractors' progress toward meeting the 10% yield and $500 unit-cost goals, the GAO withdrew a final recommendation that the secretary of defense require that these funds be used only for improving VHSIC chips' manufacturing efficiency.

Because the DOD recognizes that VHSIC chip-design changes will be necessary and the Pentagon will take control of those changes, the GAO report concludes that "the chance of a VHSIC contractor diverting yield-enhancement subsidies to other than generic design and manufacturing improvements will be minimized." *–George Leopold*

VHSIC FUNDING HAS BALLOONED ($ millions)

Funding categories	Original estimate (1981)	DOD FY85 approved (Feb. 1984)	VHSIC office revised estimate (Feb. 1984)
First-generation technology	178.3	544.9	707.1
Development and demonstration	167.8	165.5	195.5
Yield enhancement and manufacturing	–	192.0	192.0
Technology insertion	–	148.2	210.4
Other	10.5	39.2	109.2
Second-generation technology	83.6	94.2	171.2
Definition studies	–	11.3	11.3
Development and demonstration	83.6	73.0	150.0
Lithography	–	9.9	9.9
Program support	76.8	141.8	141.8
Design automation	–	62.2	62.2
Research projects	36.8	40.0	40.0
Management	40.0	39.6	39.6
Total	338.7	780.9	1,020.1

SOURCE: GENERAL ACCOUNTING OFFICE

AUTOMOTIVE

SGS CARVES NICHE IN REGULATORS

Agrate, Italy

Italy's principal maker of semiconductor components has its sights on what could be a dream niche in the automotive world. SGS Microelettronica SpA (formerly called SGS-Ates) says it has developed the world's first monolithic voltage regulator for car alternators.

Scheduled for sampling in September, the L9480 is produced in the company's Multipower-HV1 high-voltage high-power technology. It is based on a proprietary two-step ion-implantation technique that produces a small hourglass-shaped p+ isolation well. The well allows the chip to handle high voltages [*Electronics*, Sept. 8, 1982, p. 84].

The chip is a self-oscillating switching regulator that integrates the control circuitry and power section necessary to regulate the output voltage of an automotive alternator by controlling the excitation current in its field winding. It provides a cheaper, more reliable replacement for the current industry-standard solution, a three-chip (control, Darlington, and diode) hybrid. And the SGS chip requires no external components; the hybrid needs supplementary passive parts.

Perhaps the most impressive facet of the SGS chip is the size of its potential market. Antonino Milazzotto, the company's manager for bipolar automotive products, is aiming at nearly 13 million pieces per year. This figure represents 70% of the 18 million non-Japanese cars that use a simple one-function regulator, as opposed to the more complex fault-analyzing units used in many high-priced vehicles. SGS sees Japan as an impenetrable market for such devices.

Adds up. "Our target price is under $2, which will save an automobile manufacturer between 50¢ and $1.50 per car," says Milazzotto. "When you consider companies like General Motors, which produce about 4 million cars per year, that can add up."

He is also confident that the chip's specifications—it operates at 50 V and can deliver up to 4 A with protection against load-dump transients of up to 100 V—will keep the competition at bay for a while. "Most of the major bipolar-chip manufacturers have a technology capable of handling those specs," he admits. "But most of them would have to go to complex processes like dielectric isolation, and that's too expensive for this kind of application." *–Robert T. Gallagher*

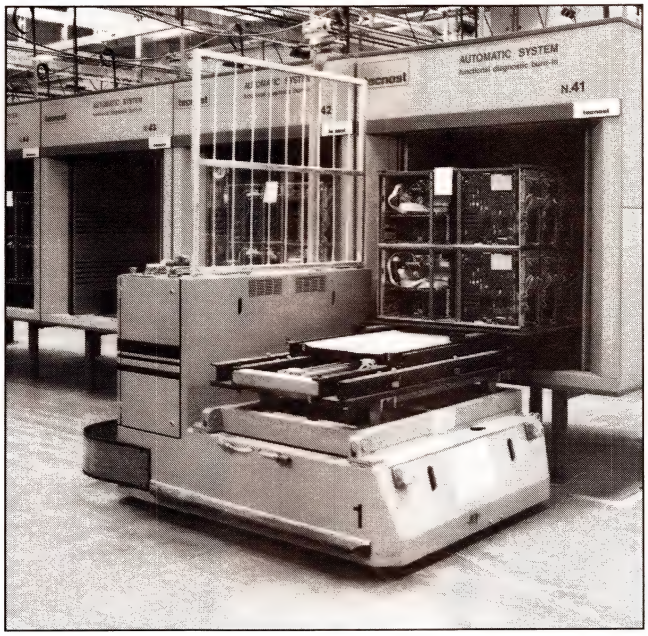
OLIVETTI AUTOMATES ITS IBM PC CHASE

Scarmagno, Italy

Italy's foremost producer of data-processing and office-automation systems hopes its new, highly cost-effective factory will give it an edge over IBM as a supplier of personal computers on both sides of the Atlantic.

Already in production, Ing. C. Olivetti & C.'s highly automated facility should have all its systems installed within three months. By then, it will be churning out machines compatible with the IBM Corp. Personal Computer at a rate faster than one per minute over two shifts per day.

This year, the factory will produce a total of 250,000 computers, the backbone of Olivetti's total scheduled production of 400,000 machines. The company considers the other 150,000 machines its marginal production, which can be expanded or reduced in response to market forces. These computers are manufactured in several other Olivetti factories.



No hands. Computer subassemblies are transported to and inserted in an Olivetti Tecnost diagnostic burn-in functional tester.

Production of IBM PC-compatibles has predictably become a commodity business rather than a value-added business. IBM asserted from the time of its entry into the microcomputer market that it would be the world's low-cost producer of personal computers based on its PC-DOS variation of the MS-DOS operating system.

Faster and cheaper. Nonetheless, Olivetti executives reckon that with their new production facility they can undercut the U.S. giant on a cost-per-function basis. The claim is supported by the fact that Olivetti's M-24 computer is significantly faster than the standard IBM PC—twice as fast for many functions—and still costs less on the open market.

Olivetti cannot keep M-24 prices artificially low for competitive reasons. The company is the sole supplier of PC compatibles to AT&T Co. and Xerox Corp., who call the M-24 their PC 6300 and the 6064/6065, respectively. Both those companies sell the Olivetti-supplied machines at prices equal to or lower than the ticket price for the standard IBM model.

Giulio Bairati, Olivetti's production process manager, attributes the factory's cost-effectiveness to two factors. First, instead of an assembly plant, it is a complete production facility. Integrated circuits, capacitors, printed-circuit boards, mountings, cases, and other components enter at one side of the building, and complete, packaged computers are shipped from the other side.

The more standard approach is to subcontract such tasks as component insertion and circuit-board test, Bairati says, leaving only final assembly for the principal manufacturer. He asserts that Olivetti's approach gives the firm more control over the production process and, consequently, over costs.

Olivetti's other money saver is automation. With most test and production equipment supplied by subsidiaries Olivetti Tecnost and Olivetti Controllo Numerico, respectively, the facility employs only 450 workers spread over two shifts to produce 72 personal computers per hour. That works out to a rate of one machine every 50 seconds or, more significantly, one computer per three hours of employee time.

Three Olivetti minicomputers control the production process, which includes an integrated system with robotic handling for automatic parts storage, inventory, and ordering; most component mounting; soldering; washing; internal transportation; and test. Only 10% of the mounting operation—dealing with components that are unsuitable for automated treatment—and the final assembly stage are handled as manual processes.

Bairati says that should Olivetti's production plans change, the facility is flexible enough to be used for the manufacture of any of the company's other products. *–Robert T. Gallagher*

JAPANESE RESEARCHERS BRIGHTEN THE EL BLUES

Tottori, Japan

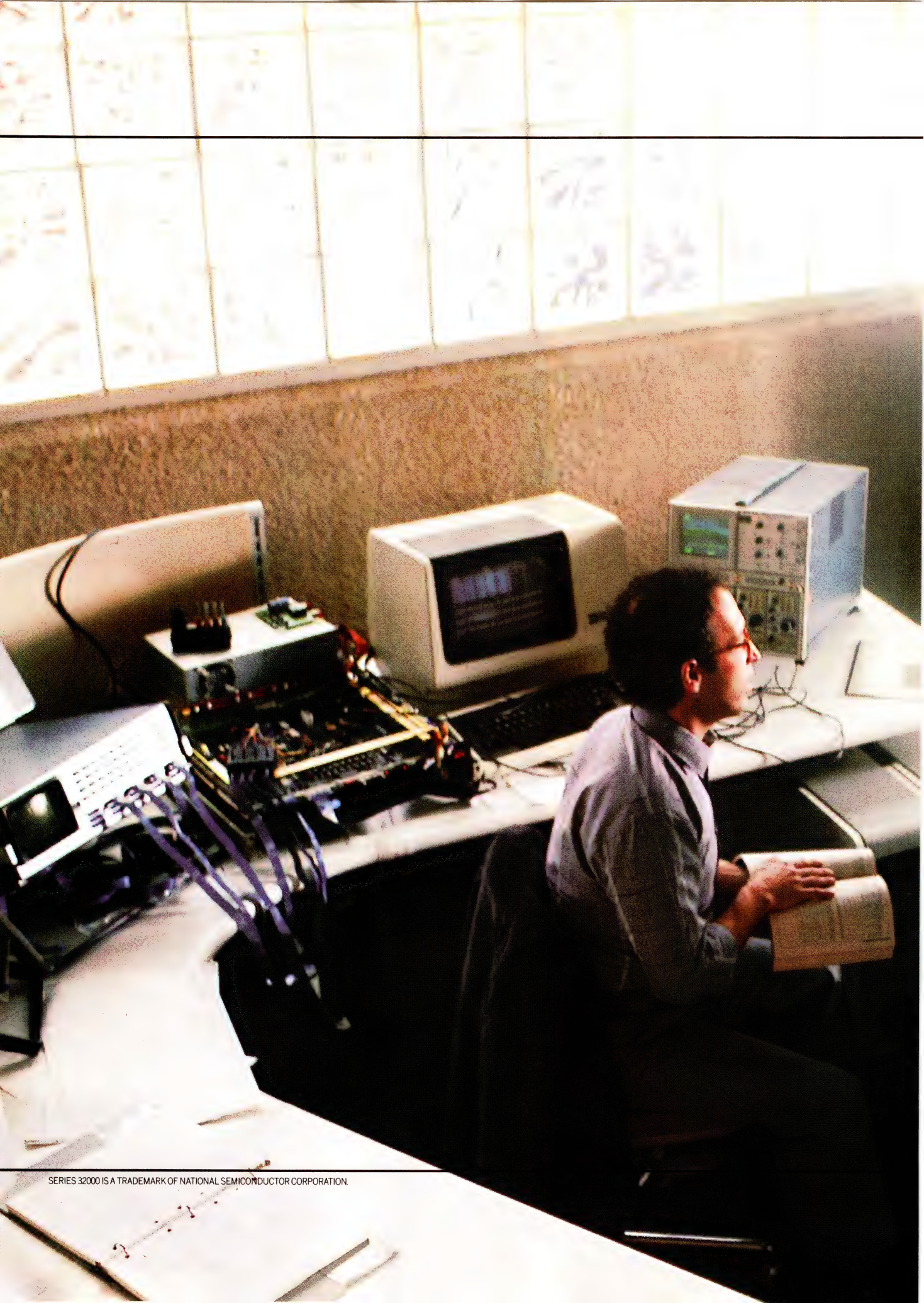
If they can keep boosting the brightness of their blue phosphors, two Tottori University professors could turn electroluminescent displays into the technology of choice for attractive, thin-panel, large-screen video displays. Hiroshi Kobayashi, Shosaku Tanaka, and coworkers have focused most of their attention on blue because they believe that developing a bright blue phosphor is the key to building full-color displays.

High-brightness yellow-hued displays are now made commercially by Sharp Corp. in Nara, Japan, and by Planar Systems Inc. in Beaverton, Ore. Applications include portable computers and such instruments as an emulator for 16-bit microprocessors from Iwatsu Electric Co. and a network/spectrum analyzer from Anritsu Electric Co.

System manufacturers install the displays because of their short depth and low power consumption, and because they don't need a high-voltage power supply. Many users find them superior to cathode-ray tubes because the nature of the EL display's matrix makes for a planar display with extremely high linearity and no dot-focusing problems.

Ironically, available EL displays cannot be used for black and white TV: their color makes them look unnatural and unattractive. The technology for producing the three primary-color phosphors for color displays, however, can be used to produce a mixed phosphor that emits white light.

The newly developed phosphors are sulfides of alkaline-earth metals doped



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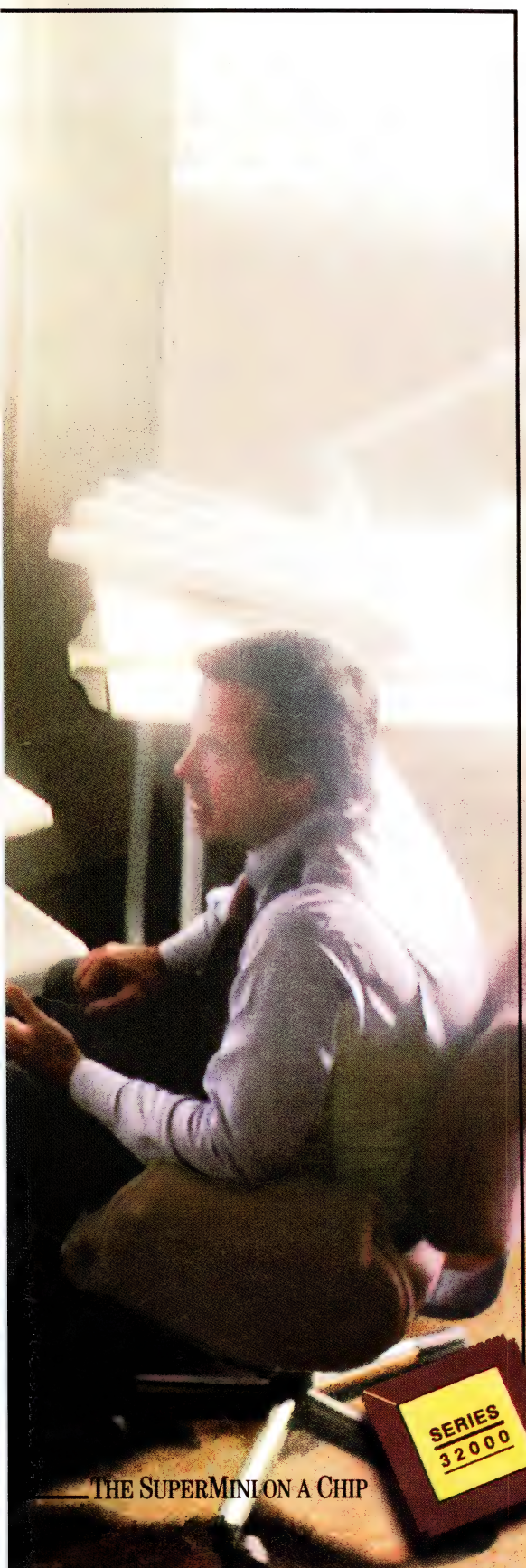

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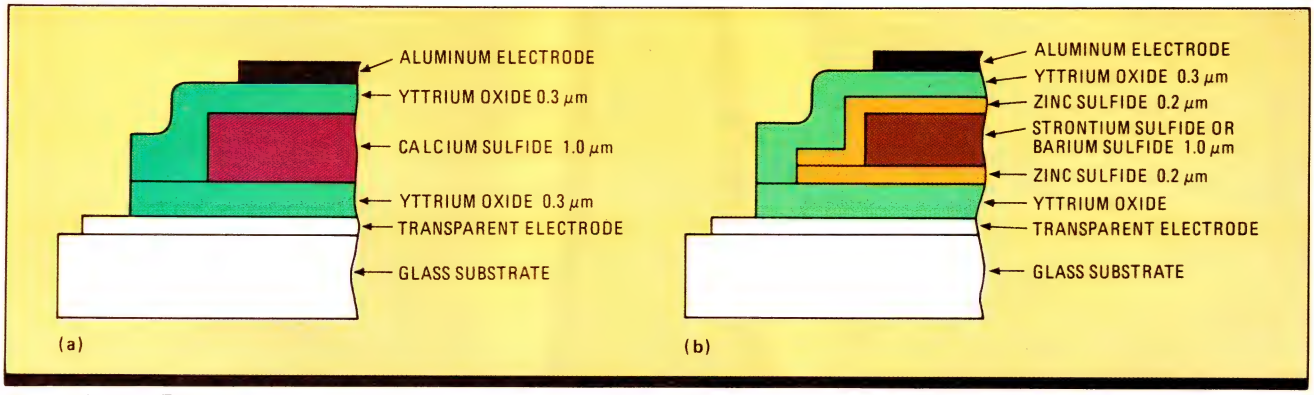


Jacket. A green EL cell (a) uses sulfide that doesn't react with Y_2O_3. But SrS in the new blue EL cell (b) does, so layers of ZnS isolate it.

with rare-earth luminescent centers, which replace the commonly used zinc sulfide doped with manganese.

The wider band gap of these materials compared with zinc sulfide and their high dielectric constant are both advantages in ac operation. Moreover, the similarity between the ionic radii of these host materials and those of the rare-earth metals that are used to activate them simplifies the incorporation of the rare earths into their lattices.

Commercial models are still some years away

The Japanese team excited the experimental EL cells with a 200-V, 5-kHz sine wave. Blue cells with a strontium sulfide phosphor activated with cerium have a reasonably high luminance of 520 cd/m^2. Green cells of calcium sulfide activated with cerium have a luminance of 650 cd/m^2, and red cells of calcium sulfide activated with europium have a luminance of 100 cd/m^2. Most effort has gone into the blue phosphor because it has been the most difficult.

Brighter greens. Green phosphors should become brighter without too much effort, the researchers say. Nor are they much worried by red, because there is an alternative method of making a bright red phosphor if one cannot be made directly: a red phosphor that fluoresces when exited by green light can be used.

Deposition temperature is also extremely important. The best results have been obtained at about 400°C. Ambient conditions during fabrication are also important, and excess sulfur appears to be important to maintain the balance of ingredients in the reaction.

The high-brightness display cells are built using the classical capacitor structure: insulating layers on either side of a phosphor separate it from the capacitor plates. A conventional structure is used: the light-emitting layer is sandwiched between two yttrium oxide layers. But when SrS is used as the emitting layer, the Y_2O_3 tends to react with it and weakens the adherence of the film to the glass substrate. To prevent this, two protecting layers of ZnS are introduced (see figure).

Although the phosphors are bright, about ten times more brightness is needed for commercial displays. This may take a number of years to accomplish. Display brightness is proportional to refresh rate, and most displays are refreshed at only 60 Hz. Development of large-area thin-film transistor arrays, which are also needed for high-contrast liquid-crystal displays, could supply the memory function needed for practical displays at the present levels of luminosity.

Plasma and EL displays offer hopes for light-emitting flat-panel displays that would be more attractive than the LCDs now used for everything from personal computers to miniature color TVs. LCDs by themselves do not emit light, and even when backlit they produce less vibrant images than other types of displays.

Although EL displays lag behind plasma types in commercialization (only two manufacturers are shipping them in quantity), their simpler, solid-state structure still offers a number of advantages. This is especially true in color panels, where the structure of EL displays is markedly simpler than that of plasma displays. *–Charles L. Cohen*

LIQUID-CRYSTAL FORMULA BREWS CRT REPLACEMENT

Harlow, England

The long-awaited replacement for the cathode-ray tube may have arrived—at least for desktop terminals, portable computers, and other products where small size and low power are more important than the rate of screen update.

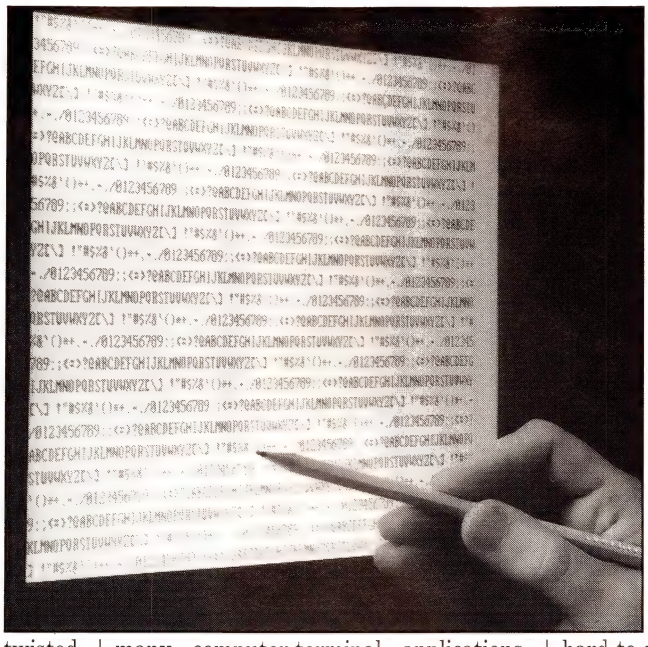
STC Technology Ltd.'s Harlow research center, Standard Telecommunications Laboratories (STL), has divulged details and photographs of a prototype smectic liquid-crystal display that matches a standard CRT's screen size and resolution. The display produces a high-contrast, flicker-free, black-on-white image and offers one advantage over the CRT—it holds data with the power off.

Smectics, a relatively unused class of liquid-crystal materials, can be switched between clear and cloudy, or with a dichroic dye, it becomes jet black. It will remain in either condition even when the power is off. One snag is that smectics are difficult to switch. It also may take years before the new display can match the CRT in price and speed. In addition, upcoming LCDs driven by thin-film transistor arrays may challenge smectic LCDs. Despite these drawbacks, STL's display may soon turn up in several products from parent STC and ITT.

ITT Courier, the U.S. manufacturer of telecommunications gear, invested in the display's development at STL to garner rights for its use in its terminals. Britain's International Computers Ltd. plc, now a subsidiary of STC plc, makes an executive work station that could use a cheap flat-screen display. And ITT Corp., a maker of computers compatible with the IBM Corp. Personal Computer, could get a jump on the market with a flat-screen laptop. Just as the small LCD won the calculator war for the Japanese over a decade ago, so too its bigger brother could be crucial to success in the portable-computer and executive work-station markets.

For the moment, though, STL will not elaborate on production commitments and will discuss only the technology, first unveiled in a paper presented at the recent Society of Information Display Conference.

In earlier smectic prototypes, lasers



Storage display. Smectic LCD technology from STC Technology Ltd. offers high contrast and a wide viewing angle. A new screen is written in 0.84 s.

and heaters, in concert with an electric field, had been used for the job: heat thaws the highly viscous smectic. Once in a watery or isotropic state, it cools, freezing into one of two optical states, determined by the presence or absence of an electric field. Designers found this a clumsy arrangement.

To get around the problem, STL developed, with the help of BDH Chemicals Ltd., a liquid-crystal cocktail that can be switched electrically, without the help of heaters. The required switching voltage is still high, however—about 300 V compared with 15 V for a twisted-nematic display.

Multiplexed. Driver electronics are expensive for most flat-panel displays. Designers can cut costs by multiplexing the electronics between display lines, but in a conventional twisted-nematic LCD, the contrast drops as more lines are added. That is because twisted-nematic displays must be permanently powered to stay on: when the driver circuitry is multiplexed, the effective signal voltage falls, and with it, the contrast between on and off states.

Thanks to the storage effect, multiplexing does not cause this problem for a smectic-based display. Once switched on, it stays on and can be indefinitely multiplexed without losing contrast. The STL prototype, for example, uses 400 : 1 multiplexing. Thus large and complex panels can be built economically.

STL's prototype has a screen measuring 7.6 by 10.1 in.; a production version would be slightly larger. Text is formatted into 25 lines, each of 80 characters, on a grid of 760 by 420 pixels—each character is built from a 9-by-16-pixel field. The black-on-white display has strikingly high contrast—better than 7 : 1—free of the flicker common to CRTs. Because the optical-switching effect does not rely on light polarization, the display can be viewed from any angle. It can be operated in passive mode or illuminated by a plastic light guide.

Prototype replaces CRT in computers but is too slow for TV

But the display is slow. A page of data can be written in 0.84 s and cleared in 40 ms. That speed is fast enough for many computer-terminal applications, but too sluggish for TV. STL researchers believe they can narrow that gap—and even add color—but other observers are not so sure.

Modern integrated-circuit drivers can deliver the voltage needed to switch STL's smectic A compound. Bell Telephone Manufacturing SA, a Belgian subsidiary of ITT Corp., has designed a 30-channel display driver that switches ±150 V. This custom-designed 27-mm² chip, says STL, could be shrunk to 15 mm². The panel's driver ICs draw 5 W in the page-dump mode and 2 W when writing to the screen at 8 characters/s. These figures sound high, but the average power use is lower—the display uses no power at all when new data is not being written.

The driver chips are tape bonded to the glass substrate, and a silicon rubber encapsulates the chip area. The setup eliminates over 1,120 external connections.

A current favorite among technologies competing with STL's display—the LCD driven by thin-film transistors integral with the array—is proving hard to make: it is difficult to get all the transistors working. In addition, the double-layer metallization needed makes it less reliable (Britain's Hirst Research Center has a planar process in the works). A strong challenger may yet emerge in the flat-panel competition. But for now, the STL display appears to be the nearest thing yet to a replacement for the CRT. *–Kevin Smith*

TELEVISION

ITT READIES DIGITAL CHIPS FOR U.S. STEREO TVs

Freiburg, West Germany

The ITT Semiconductors Group, which pioneered digital TV, is doing what comes naturally now that stereo-sound TV is on the rise in the U.S. The company is readying a pair of digital chips for processing audio signals in NTSC color receivers.

The two-chip set is designed for the de facto U.S. standard for stereo-sound TV transmission—the multichannel-TV-sound (MTS) system developed by Zenith Electronics Corp. and the DBX division of BSR International (USA) Ltd. One chip is an audio processor very much like the one ITT designed for West German stereo-TV receivers, so the German firm got off to a fast start. It has already delivered samples to an as-yet-undisclosed U.S. set maker.

Developed at Freiburg-based Intermetall GmbH, lead house of the ITT Semiconductors Group, the two chips represent the first digital approach to audio signal processing for the MTS system, according to Edmund Zähringer, leader of the project at the company's Concept Engineering Department. So far, only analog solutions have been used in U.S. stereo TV receivers. (Stereo TV broadcasts in the U.S. began with last year's Summer Olympics in Los Angeles.)

As in video processing, the digital chips offer substantial advantages to both set makers and viewers [*Electronics Week*, Aug. 13, 1984, p. 53]. Still, Zähringer is at a loss to estimate the U.S. market for them. It all depends on how influential the industry is in getting the major networks to go all out for multichannel audio, he says. "But we believe the U.S. market will become a substantial one for us, and we are prepared for large-volume deliveries of our chips."

Multiplexed signal. The Zenith-DBX system modulates an FM signal onto the 4.5-MHz audio carrier. This signal encompasses the main left-and-right stereo channel, a stereophonic subchannel, a secondary audio program (SAP) subchannel, an engineering channel, and a pilot subcarrier. The multiplex signal spans a range of about 100 kHz.

The SAP subchannel allows a TV viewer to listen to a program in the original language or to the same pro-

gram in another language. The engineering channel not used for programming is for sending data from a main broadcast station to other transmitters in the network, among other uses. Signal-compression techniques are used at the transmitting end to reduce noise in the stereophonic and SAP subchannels.

Converter and processor. To process the multiplex signal, ITT designers chose to use an analog-to-digital converter, the ADC2300U, and an audio processor unit, the APU2400U. Expansion of the already compressed stereophonic and SAP subchannel signals must still be performed with the set maker's own (analog) circuitry. "But we are now working on a digital expander," Zähringer says. "Off-line simulations have already been completed."

Two-chip set fits Zenith-DBX system standard

The converter chip is a large-scale integrated circuit that uses ITT's proprietary collector-implanted high-density bipolar technology. It integrates source switches, demodulators, ADCs, and detectors on a 7.4-mm^2 chip.

The audio processor chip, a 33-mm^2 very large-scale n-MOS IC, packs a programmable digital signal processor and hardwired digital filters as well as digital-to-analog converters. It extracts the pilot carrier from the transmitted signal to operate the left-minus-right demodulator, and evaluates the signal for the presence of the pilot to distinguish between stereo and bilingual broadcasts.

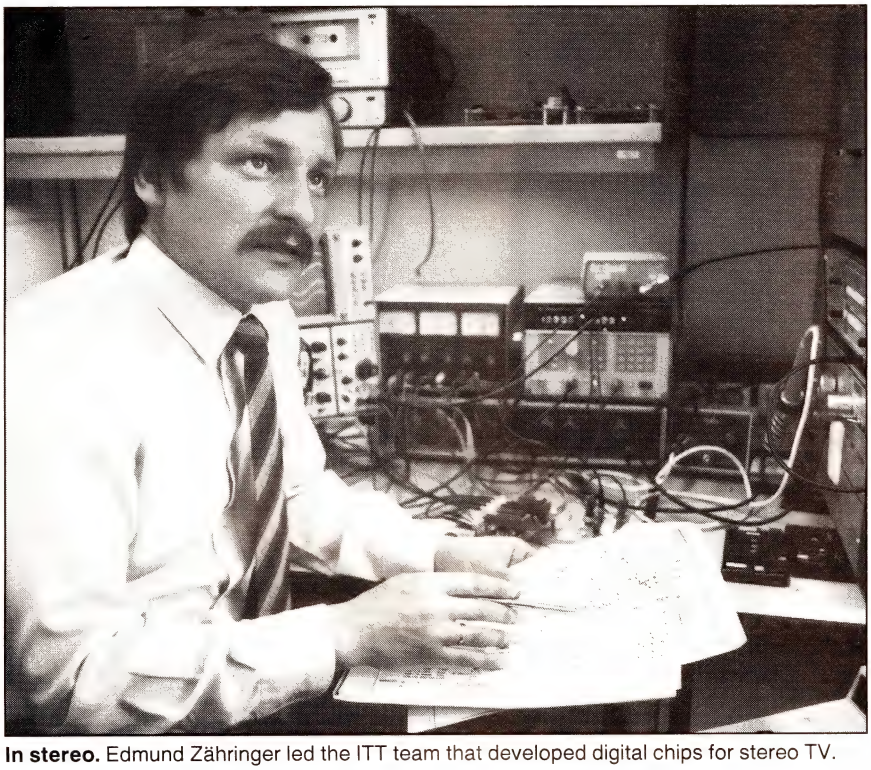
To process the audio, the source switches on the converter chip (which the user activates from the control panel) to select the analog signals—either from the receiver's intermediate-frequency stage or from a local source such as a video tape recorder—and feed them to pulse-density modulators. Performing the first step of the conversion process, these modulators put out 1-bit data streams at a rate of about 7 MHz.

The data then goes to the audio processor chip, where digital filters perform the second step of conversion. (The filters are on the audio processor chip because they can be more readily integrated in n-MOS than in the bipolar technology employed for the converter chip.)

The output of the whole ADC system is a data stream with a signal-to-noise ratio comparable to that of a conventional 13-bit converter.

The stream is passed to the audio processor chip, where low-pass digital filters suppress unwanted frequencies. This allows reducing the sampling rate from 7 MHz to 32 kHz, a rate that the chip's software can handle.

Then the data streams enter the processor's core, a programmable digital real-time signal processor with a modified Harvard structure. It performs such functions as dematrixing, deemphasis, stereo identification, and imaging, as well as bass, treble, balance, and volume control. Finally, the data streams go to DACs, where they are processed into signals suitable for driving a pair of output power amplifiers for the loudspeakers. *–John Gosch*



In stereo. Edmund Zähringer led the ITT team that developed digital chips for stereo TV.

NEWS BRIEFS

AT&T OPENS PLANT IN SINGAPORE

Chasing tax incentives, AT&T Co. is going to Singapore to produce telephones for the U.S. market. The telecommunications giant will sink $32 million over the next five years into the new factory. James Bercaw, consumer products executive president, announced in early July that the new factory, to be called AT&T Consumer Products pte Ltd., will produce 1 million telephones in its first year of operation. Plans call for the factory to reach a minimum annual production of 3 million phones by 1987.

Assembly, wiring, and testing of the telephones will be done in the Singapore factory, which will create about 1,000 jobs for Singaporeans and generate $30 million worth of local spinoff business. This move marks the first time AT&T has started a plant from scratch outside the U.S., and the factory will be AT&T's first wholly owned manufacturing facility for home telephones outside the U.S. This is the second big investment by AT&T in Singapore. Two months ago, the group paid $36 million for the manufacturing operations of Honeywell Synertek, a semiconductor firm.

Singapore's economic development board has been wooing major foreign investors, and the local AT&T plant will receive pioneer status, tax holidays, and other incentives.

HP BEEFS UP CAE LINE WITH 68020, OPTIONS

An engineering work station with a choice of processors in a flexible modular design signals a new commitment by Hewlett-Packard Co. to the computer-aided-engineering market. Filling in a medium- to high-performance gap in HP's 9000 product family, the 300 series announced today is one of the first technical work stations available that uses a full 32-bit Motorola 68020 microprocessor. The 300 has central-processing-unit, display, and memory options. The basic configuration can be upgraded, the company says.

Besides the 16.6-MHz 68020, which comes on a board with a 16-K high-speed cache and a 12.5-MHz 68881 coprocessor for floating-point performance, buyers can order the 300 with a 10-MHz Motorola 68010 microprocessor. The standard 68010 CPU board holds 1 megabyte of RAM, and memory can be expanded up to 7.5 megabytes.

The series 300, which will run most of the applications written for the series 200 68000-based work station, is primarily for instrument-control and technical-design applications.

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CAN U.S. CHIP MAKERS SUCCEED IN THE JAPANESE MARKETPLACE?

by Michael Berger

'INCREDIBLE WEB' OF JAPANESE RELATIONSHIPS WILL PREVENT AMERICANS FROM INCREASING THEIR 10% MARKET SHARE

American semiconductor makers still dominate the largest market in the world—their own. But in the No. 2 market, Japan, their share is "about 10%, and slipping," as a veteran U.S. executive in Tokyo puts it.

"It doesn't mean we aren't making money," he adds. "We are, and we expect solid growth once this flat market turns up again. But as for the overall position here, I just can't see it growing."

The reasons why U.S. firms cannot make headway have little to do with formal market barriers, company executives say. Semiconductor tariffs on all products of major interest to U.S. firms have been eliminated, thanks to legislation by both governments, and specialists at the U.S. embassy in Tokyo say they have seen no evidence of Japanese makers violating the law to keep out foreign competition.

What is holding back foreign sales is what one American calls "the incredible web" of interlocking relationships upon which so much business in Japan is based. "Is the market closed because sellers at Matsushita and buyers at Sony went to school together and won't break up their business relationship for some American supplier who comes in with a competitive price?" asks another U.S. executive, who asked not to be identified. "I don't think so. But it is a market that takes a helluva lot of massaging."

Even that doesn't always pay off. One U.S. chipmaker, seeking to broaden its Japanese sales base, brought over a vice president last year to pledge its commitment to an important new customer. "They vowed to use us for life," says the firm's Tokyo representative. "But 'life' turned out to be six months. When the market turned down, they even tried to return our products."

The American role could have turned out differently. U.S. firms could have gained a major foothold 15 or 20 years ago—albeit on terms dictated by Japan's Ministry of International Trade and Industry. The Japanese government had embarked on a campaign to upgrade the nation's semiconductor industry by acquiring the latest technology. Its policies allowed foreign companies to enter by way of joint ventures with Japanese partners. U.S. companies deemed the ministry's conditions too troublesome, however, and were virtually shut out, except for Texas Instruments Inc. (see "TI guns down the opposition," p. 32).

Other hidden barriers remain. These can take the form of Japanese engineers who find it easier to reject a foreign product that tests out improperly or Japanese companies cutting orders to their U.S. suppliers when foreign customers reduce their inventories.

Not enough U.S. firms are manufacturing in Japan

The most common complaint of the U.S. chip makers, in fact, is that they often are treated by their Japanese customers as little more than peripheral suppliers. "We rarely get a chance to get into that inner circle which characterizes most supplier-customer relationships here," says a U.S. executive. "But I can't afford to say that publicly, because it would jeopardize the relationships our company has been able to build. How do we overcome this barrier? You tell me—I've been trying to do just that for more than three years."

Costly solution. As formidable as the market barriers are, there is a strategy—an expensive one—to attack them: build a plant in Japan. "U.S. technology in most semiconductor products is still very competitive, but in a fiercely competitive market like Japan, you've got to have a substantial presence here to win," says Richard May, a trade counselor at the U.S. embassy in Tokyo and a former Dataquest Inc. researcher in Japan. "A sales office isn't enough. We still don't see enough American firms manufacturing in Japan."

At least one firm has followed that path. TI now has four plants in Japan, three of which make semiconductors. Its latest, in Miho, is a twin of the Dallas front end that makes 1-Mb dynamic random-access memories.

Other industry sources in Tokyo argue that the only way to control the advantage that Japanese manufacturers have in the trade balance of integrated circuits (see chart, p. 33) is for U.S. firms to adopt a basic military tactic and attack from the rear: take on the Japanese on their own turf. "Tie them up a bit here in Japan, and they'll have to divert resources to take you on," says one American. "Right now, they aren't taking us very seriously, and the only way they will is if we make or design product here."

U.S. trade counselor May doesn't recommend producing mass-memory products in Japan—"Japanese production economies of scale are just too strong," he concedes—but he argues that basing manufacturing or design centers for other products in Japan has multiple payoffs. "It's more than just selling your product," he says. "It's being part of the Japanese research and development scene and thus attracting good young engineering talent. But you can't do that with just a sales office."

Too expensive. The response to this argument is that producing in Japan is simply too expensive. "In America, we have 30- to 90-day marketing plans," says James R. McGrath, representative director of Monolithic Memories Inc. Japan. "In Japan, they have 3- to 5-year plans. You have to show them you have a solid, long-term commitment in this market to succeed here."

But beyond informal barriers and U.S. systemic weaknesses are even more daunting Japanese strengths, such as the lower cost of borrowing money and the vertical integration of the major Japanese electric companies. With these factors, the Japanese can absorb losses and marshal forces in a way no U.S. maker but IBM can even consider.

"There are no Japanese semiconduc-

tor companies," says a veteran American semiconductor industry executive. "There are only Japanese semiconductor operations, buried in the bowels of their massive electric companies. Moreover, most of those semiconductor operations, especially under present market conditions, do not make a profit, because they don't really have to."

When NEC Corp., Hitachi Ltd., or the other major Japanese semiconductor makers engage in marketing and product planning, it is within the secure framework of a conglomerate. The security is further reinforced by long-standing links to banking groups.

Fewer worries. The major banks, knowing that the future strength and vitality of the Japanese economy rests largely with the electronics companies, have fewer worries about the solvency of these firms, because the banks themselves and their cash supply are part of each company's financial infrastructure. This is in sharp contrast to the plight of U.S. semiconductor makers, who are forced to deal with banks whose primary interest is not the future of the national economy, but return on investment.

These factors, as much as the daily problems of doing business overseas, lead Americans in Tokyo to question their ability to become a significant factor in that market.

What the U.S. chip-maker representatives do see, though, are opportunities to build on their combined 1984 Japanese sales, which were estimated by market analysts at close to $600 million. U.S. companies in Japan are using three basic marketing approaches.

Three options. One is to compete in mass products, as Texas Instruments Japan Ltd. is doing with its Japanese production facilities. Another is to capitalize on patented technology, as Nippon Motorola Co. and Intel Japan Corp. are doing with their microprocessors and other products. The third approach is to go for specialized niche markets, such as Monolithic Memories' patented programmable-array-logic circuits, National Semiconductor Japan Ltd.'s programmable-logic and hard-disk chip-set products, and Advanced Micro Devices Japan Inc.'s upper-end memory products.

The third approach is the most popular, since most U.S. companies have not chosen to make the sizable investments necessary to produce in Japan. It's also the third best approach strictly from the revenue angle: the major U.S. money-makers in Japan are TI, Intel, and Motorola, who either produce in Japan or have technology the Japanese cannot yet match.

Like TI, Motorola has a production plant in operation, and a third company will join them early next year. Fairchild Camera & Instrument Corp.'s Japan office is investing a reported $40 million to install production facilities for the integrated manufacture of 64-K DRAMs at its plant in Isahaya. Fairchild has been assembling and testing ICs at its plant since May 1984, and also plans to mass-produce 64-K static-RAM and gate-array products by 1987.

In addition, NCR Corp. announced recently it has organized a semiconductor division at its Oiso plant to produce electrically erasable read-only memories, 32-bit processors, and peripheral large-scale chips for its Small Computer System Interface. Operations will begin early next year.

Tokyo base. Most other U.S. firms in Japan are using Tokyo area sales and design centers as their basis of operations. But by far the largest design center is Intel's at Tsukuba, site of Japan's Science Expo, where the company customizes its microprocessor and EEPROM products. There has been talk of production in Japan, and Intel has plen-

TI GUNS DOWN THE OPPOSITION

Texas Instruments Japan Ltd. has achieved its solid position in the world's second-largest semiconductor market for one basic reason, says an executive at a rival company: "TI had a loaded gun and used it." The gun was TI's strong patent position in the early 1970s, when the Japanese were starting their game of technological catch-up with one rule: if you have technology we want, and you want to get into our market, you'll have to do it through a joint venture.

But in the late 1960s, Fairchild Camera & Instrument Corp. built a small transistor plant in Okinawa, which was still under U.S. military control. It planned to enter the Japanese market automatically when Okinawa reverted to Japanese control in 1971, but the Japanese realized that the Palo Alto firm's technology was no longer on the leading edge, and backed off. A Fairchild-TDK joint venture was dissolved in 1978.

TI was in a much stronger position, but it still had to pay a price. MITI suggested a *pro forma* joint venture with Sony Corp. and forced TI to license its basic technology to major Japanese makers. But in return, the U.S. company got to phase out the Sony tie-up and open independent manufacturing operations in 1973.

TI Japan now has four plants and more than 5,000 workers turning out bipolar, MOS memory, and MOS logic products, about 80% of which are sold in Japan. Sales results last year were its most impressive yet. TI Japan president Akira Ishikawa would not reveal numbers, but says that business increased 60%. Analysts estimate that TI Japan's sales alone last year were close to $320 million, with perhaps another $80 million in export sales. "This year will probably be flat, but in our 17 years in Japan, we have averaged 21% annual growth, and that is our goal for the next decade," he says.

Getting its own production facilities in Japan, was the key to the company's success. "It doesn't always make sense. The volume in the niche markets can't justify it. But for our goals, to produce mass-market products, it was a must." TI Japan's customer base has broadened in the last three years from about 1,000 to more than 1,200, he says. Five years ago, about 20 customers accounted for roughly 70% of all TI Japan sales. Today, that figure is down to 50%.

Ishikawa sees the slump lasting until at least early 1986. So early last fall, when inventories began piling up, he called for a gradual easing of the company's seven-day, 24-hour schedule: it went down to five days. TI has not laid off any workers. "That way, when the upturn does come, we'll be able to increase production rapidly." And then, he predicts, TI Japan will be looking at another period of 20% annual growth. **–M. B.**

Results. TI Japan president Akira Ishikawa says business increased 60% last year.

ty of space at its site for a plant, but no plans have yet been announced. Further revenues for both Intel and Motorola come from licensing their microprocessor families.

Yet another U.S. maker, Advanced Micro Devices Inc., has signed production and marketing agreements with an emerging Korean operation, Gold Star Semiconductor Co. Some market analysts in Japan predict that AMD's strategy is to "make products by the carload in Korea and ship 'em to Japan." An AMD spokesman denies this, pointing to the company's ranking behind TI, Intel, and Motorola as the fourth-largest foreign supplier to the Japanese market.

Seeking niches. The rest—Signetics Japan Ltd., for example—look for niches and try to fill them. Niche-seeking, in fact, is a much broader trend. Application-specific ICs such as standard-cell or full-custom products continue to show strong growth worldwide, says analyst Robert E. Johnson of W.I. Carr (America), and U.S. companies seeking to hold their present technological edge in these products will find them increasingly attractive.

Signetics, known worldwide as a supplier of digital chips to the computer industry, is better known in Japan as a maker of Dolby noise-reduction ICs, which at one time was 60% of its business. Now it is going after another niche—programmable logic, in which it has been a leading developer.

But because the Japanese market for this product is just developing, Signetics believes staff members must invest the time to educate customers before sales will begin to take off. Nonetheless, the company, which claims about 5% of Signetics' world sales, has doubled its Japan business in the last four years.

Doing the same kind of educating with its Japanese clients that use PALs is MMI Japan. Seminars backed by a staff of 50 Japanese (nearly triple the staff MMI had three years ago) support the company's efforts to build its Japan sales to 10% of its 1984 world total of $187 million.

Another niche-seeker is Asahi Microsystems Inc., a joint venture of Gould AMI Semiconductors, Santa Clara, Calif., and Asahi Chemical Industry Co. Asahi Microsystems has established a Tokyo design center to serve its custom gate-array clients. "This is a deliberate attempt on our part to change from a standard-product company to an application-specific company," says AMI general manager Felix Rosengarten. And to establish itself in what he calls the world's most competitive market, AMI is expanding its Tokyo testing facilities.

MMI is realistic about the market and its prospects, which at the moment accounts for less than 10% of the company's worldwide business. Speaking from corporate headquarters in Santa Clara, Calif., marketing vice president Timothy Propeck says that number won't go up unless there are some fundamental changes in the structure of the market.

The Japanese have a strong tendency to buy U.S. products only if what they want isn't produced locally, he says. And as soon as it is produced locally, revenues for American companies drop dramatically. "They're pretty aggressive about getting after market areas," says Propeck. "There aren't too many sizable ones they aren't already addressing themselves."

U.S. executives emphasize that selling to the Japanese home market requires a considerable investment in time and money. "Certainly for us it does," Propeck says. "It's a difficult market to crack into. You're dealing with a fundamental 'buy homegrown products' mentality and it's tough to get past that."

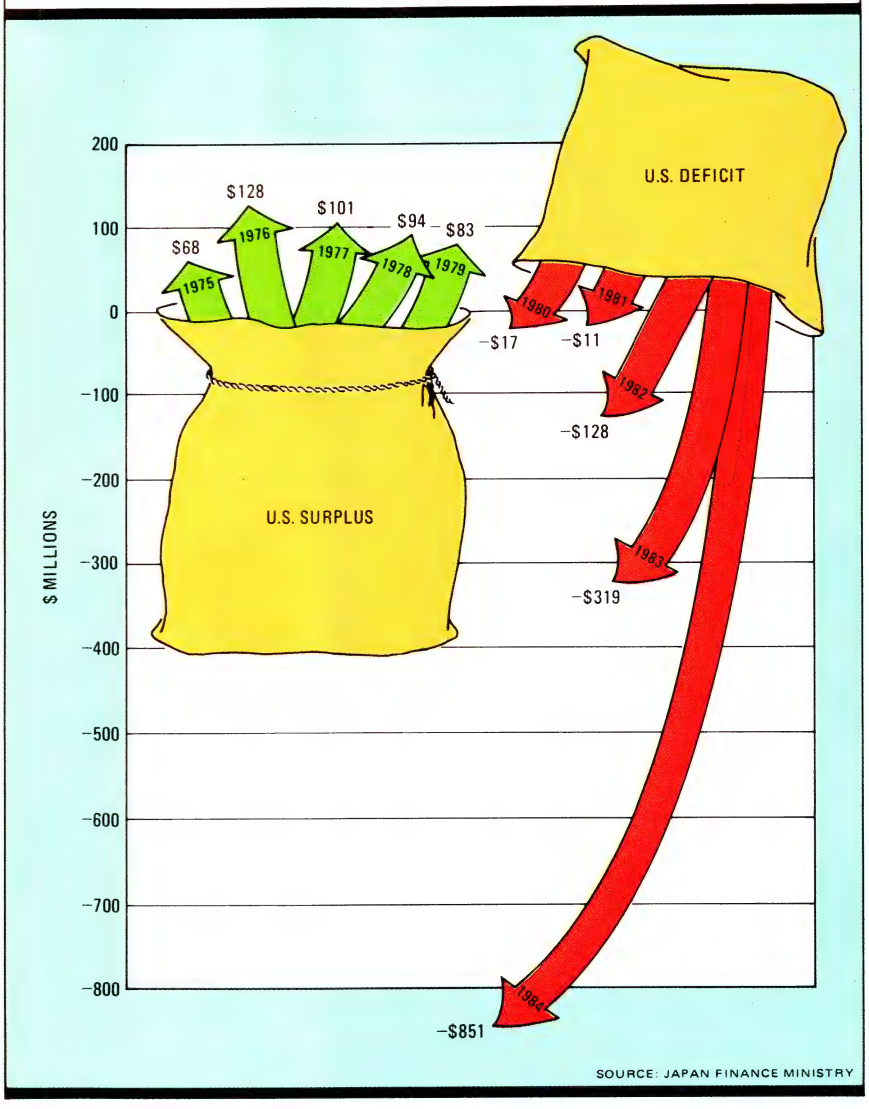
Propeck thinks the overall distribution setup is tougher to deal with, too. "They tend to have lots of different distributors that participate in the business. To sell, you have to play by that set of rules. The distributors are more or less defined by what companies you're trying to sell to.

"It's more of a fragmented distribution channel than exists elsewhere in the world," Propeck continues. "It increases support you have to provide and also increases the degree of difficulty to penetrate the market."

Meanwhile, the bottom line for U.S. makers, despite barriers both Japanese and American and the built-in advantages for native players, is growth in sales, if not market share. "We're projecting 27% growth for our fiscal year ending next March," says William G. Watson, president of National Semiconductor Japan. "And we see strong long-term growth over the next three years in our 32-bit microprocessor family."

Watson would not comment on his company's other plans, but it is believed that National is seriously considering making the ultimate commitment: a manufacturing plant in Japan. □

U.S.-JAPAN IC TRADE BALANCE KEEPS WORSENING



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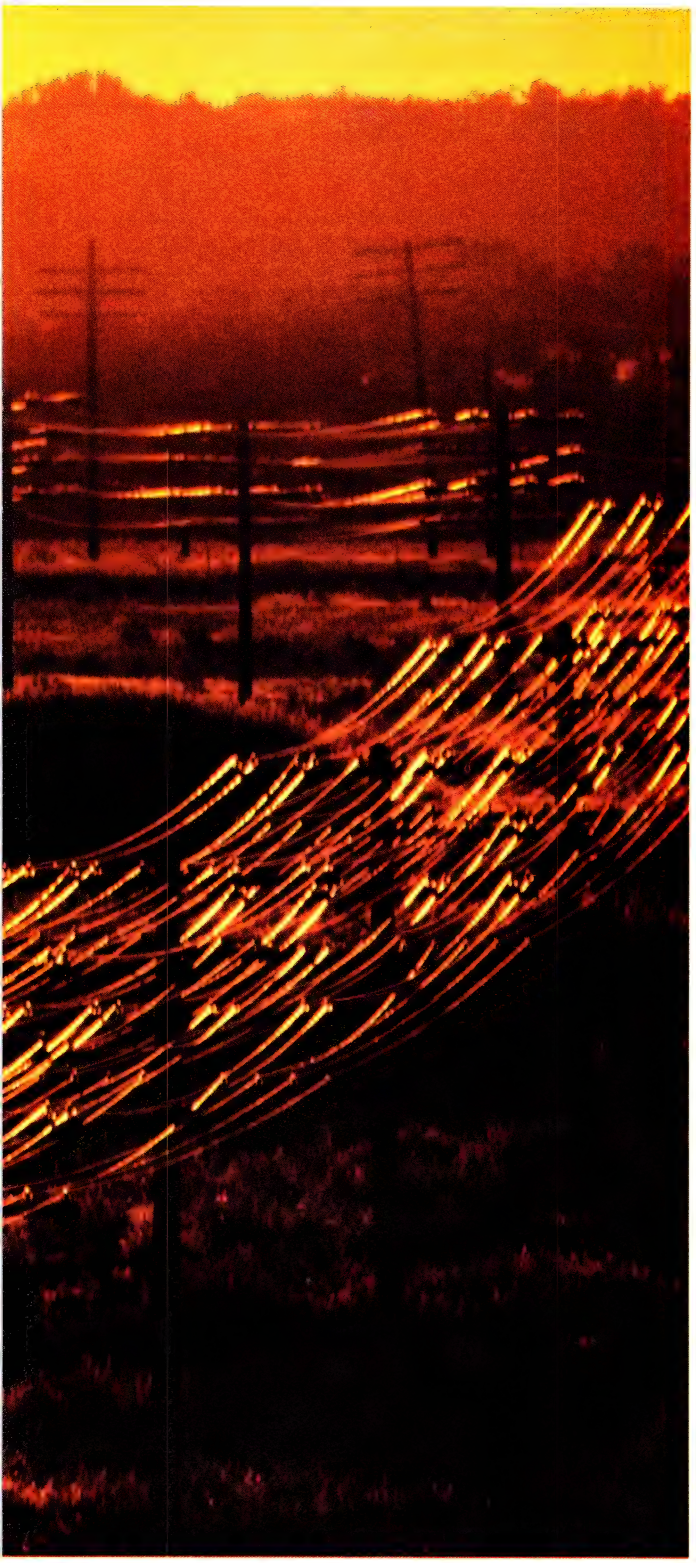

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TIGHTER VLSI GEOMETRIES CREATE PROBLEMS WITH HOT CARRIERS

by Charles L. Cohen

AS FINE-LINE LITHOGRAPHY ADVANCES, JAPANESE MODIFY LIGHTLY DOPED DRAINS TO STRETCH CHIP LIFE

Kawasaki, Japan

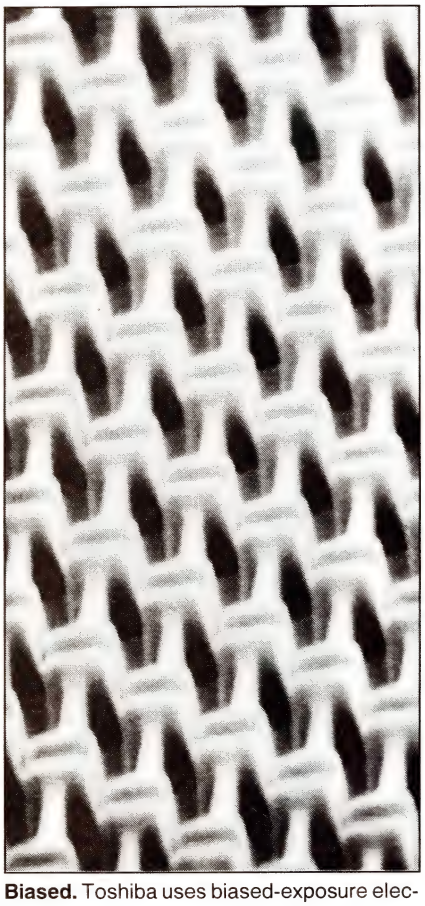
Designers of very large-scale-integration chips face a dilemma. They want to pack more and more elements into the same amount of silicon real estate to get higher yields and operating speeds. Much progress is being made in the fine-line lithography necessary for tightly packed chips. But the very fine lines create another problem: in submicron structures, hot carriers are injected into the gate oxide, and this shortens device life.

Use of lightly doped drains (LDDs) can suppress hot-carrier injection, particularly for chips that have not been shrunk below 1.2-μm line widths. But integrated-circuit researchers have found that the increase in longevity has not been as great as expected. What's more, they have learned that substrate current, generally considered a measure of life-shortening hot-carrier injection, is not a true indicator of degradation.

Two research groups at Toshiba's Semiconductor Device Engineering Laboratory here are moving rapidly toward solutions. Both are using modified LDD structures to stretch device life rather than resorting to operation at voltages lower than the conventional 5 V.

Some chip makers might have to adopt this solution—3.3 V is a commonly mentioned value—as dimensions become smaller. But it is being postponed as long as possible. Dynamic random-access-memory chips are more prone to soft errors at lower voltages, and interfacing with standard 5-V devices is difficult. (Researchers at Hitachi, IBM, and the Atsugi Electrical Communication Laboratory of Nippon Telegraph & Telephone Co. have tried a compromise solution: they use an on-chip reduced-voltage supply for internal circuits while retaining 5 V for input and output.)

One research group at Toshiba, headed by Masaaki Kinugawa, a researcher in the CMOS Memory Group, is developing devices with moderately lightly doped drains (MLDD) that have a lifetime five orders of magnitude greater than conventional LDD devices. This group also proposes a physical model for degradation and shows that degradation is not truly indicated by substrate current as commonly thought. LDD transistors tend to inject hot carriers under the space off the edge of the gate where they give rise to a depletion region not under control of the gate. In this way, both channel current and transconductance are decreased, degrading device performance. With the MLDD devices, hot carriers are injected under the gate, which retains control of channel current.



Biased. Toshiba uses biased-exposure electron-beam lithography for a 64-Mb DRAM.

The group has fabricated conventional MOS FETs that use drain implants of 3×10^{15} negative ions/cm^2. These devices have the shortest lifetime and suffer from other short-channel effects. The MLDD devices have implants ranging from 4×10^{13}/cm^2 to 1×10^{14}/cm^2. These devices have the best lifetime, retain good drivability (the ability to drive other circuits, especially capacitive loads), and sufficiently suppress short-channel effects. The LDD devices have implants of 1×10^{13}/cm^2 to 2×10^{13}/cm^2. Lifetime falls between the first two sets of devices, but the low conductivity reduces drivability.

The other team, under Yoshiaki Toyoshima of the Advanced Device Technology Group, is developing a profiled lightly doped drain (PLDD) obtained by a double diffusion of phosphorus and arsenic (with a lower concentration of phosphorus than arsenic). This configuration allows separate control of hot-carrier generation and the surface depletion region at the expense of a slight increase in process complexity.

This process uses the difference in the diffusion constants of phosphorus and arsenic, with the constant of phosphorus being higher than that of arsenic. Despite their lower concentration, the phosphorus ions diffuse further under the gate than the arsenic ions and provide the effective LDD that suppresses hot-carrier injection and short-channel effects. The arsenic ions behind them provide a moderately doped drain between the edge of the heavily doped drain implant and the edge of the gate. This controls the surface depletion region and maintains drivability.

Limit approaches. As the device researchers strive to counter the adverse effects of hot carriers in fine-line structures, the optical-lithography people press on toward even-finer lines. Optical lithography will reach a limit of about 0.4 μm in the lab and 0.5 μm in industrial production before the end of this decade, according to Makoto Nakase, a senior researcher at the Toshiba VLSI Research Center here. Nakase's prediction, made at the Society of Photo-Optical Instrumentation Engineers' Conference in

Santa Clara, Calif., last March, is based on an argon fluorine excimer laser operating at a wavelength of 0.193 μm.

Yutaka Hayashi, head of the Semiconductor Device Section of the government's Electrotechnical Laboratory, gives a more optimistic limit for optical systems in the laboratory: 1.5 times the wavelength of the light source, or 0.3 μm for a 0.193-μm source. He says that sources of shorter-wavelength light could be developed in the future to further reduce the dimensions at which optical systems can be used.

In addition to those groups in Japan that are increasing optically obtainable resolution, most other major firms in Japan—including Hitachi, NEC, and Fujitsu—are doing preliminary work with X rays. Lack of proper equipment have hampered early efforts, a situation that should change in the near future when Nippon Kogaku begins selling X-ray aligners. In the U.S., Perkin-Elmer and Micronics (using technology from AT&T Bell Laboratories) are also developing X-ray aligners.

A give-and-take. Optical step-and-repeat lithography that uses masks made by electron-beam pattern generators remains the choice for high-speed production. X-ray lithography offers the promise of similar capabilities at wavelengths that are much shorter than the smallest device dimensions. Electron- and ion-beam techniques make the finest patterns because they neither require masks nor suffer from the wavelength limitations. Unfortunately, beams must scan the pattern, and throughput suffers.

Steppers that are now used to make VLSI chips with a minimum feature size of 1.2 or 1.3 μm commonly use the mercury vapor lamp g line at 0.436 μm and a trilevel resist for increased contrast. But the limit of practical resolution is about 1 μm. Norio Hasegawa, an engineer in the 3rd Department at Hitachi's Central Research Laboratory in Tokyo, is using the mercury vapor lamp i line at 0.365 μm to resolve hole diameters as small as 0.7 μm, and even smaller line widths. He says that the equipment is suitable for production of the coming generation of 4-Mb DRAMs with 0.75-μm line widths.

Toshiyuki Horiuchi, at the Atsugi ECL, has performed a detailed analysis of an i-line stepper with separate apertures for controlling numerical aperture and illumination coherency. Horiuchi, a staff engineer in the Microfabrication Systems Section, has fabricated patterns with minimum widths as small as 0.6 μm at rates as high as 45 4-in. wafers an hour.

Masaru Sasago, at the Semiconductor Research Center of Matsushita Electric Industrial Co., in Osaka, teams the mercury vapor i line and optical contrast-enhanced lithography to produce 0.6-μm patterns. GE and Toshiba pioneered the use of photobleachable contrast-enhancement layers on conventional photoresists to produce high-contrast fine patterns. The Matsushita researchers add a new twist by using a water-soluble photobleachable material (see figure). The enhancement layer cannot intermix with the resist layer. There is no need for a special organic solvent to remove the enhancement layer.

For higher-speed lithography at linewidths below 0.5 μm, Kimiyoshi Deguchi, a staff engineer in the Patterning Section of the Integration Process Technology Development Division at the Atsugi ECL, has developed a hybrid system that combines step-and-repeat X-ray lithography with a optical stepper that performs 10 : 1 reduction. X-ray lithography is used for the 0.3-μm gates and contact holes, which have the finest dimensions of all the elements on the chip. Photolithography is used for other features. Electron-beam pattern generators draw X-ray masks that are aligned with photo-replicated patterns to maintain accurate alignment.

At Mitsubishi Electric Corp., Tadao Kato developed a simple technique using a focused ion beam, which does not suffer from proximity effects. Kato manages the EB Lithography Technology Group, LSI Process Development Department 1, at the company's LSI research and development laboratory in Itami. Gallium ions implanted into the photoresist are converted into gallium oxide, which resists oxygen plasma in a reactive ion etcher; the plasma removes the unimplanted resist. The technique has been used to fabricate gates with lengths of 0.3 to 0.8 μm on n-MOS FETs. All other lithography steps were done with optical printing, using a conventional 5 : 1 reduction.

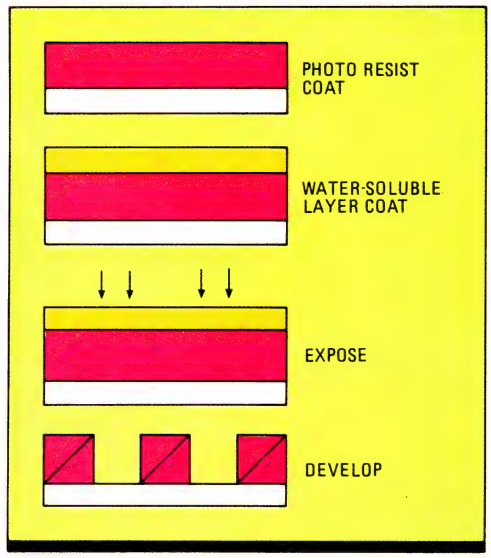
Most Japanese firms are looking to X-ray lithography

At Toshiba, Tadahiro Takigawa and coworkers are taking aim at the 0.25-μm line widths that will be necessary for 64-Mb DRAMs. Takigawa, who is senior researcher in the Basic Research Department, thinks he has developed the simplest method of eliminating the electron-beam proximity effect. Prior to lithography, the resist layer on the chip is given a bias exposure that by itself cannot be developed.

With standard electron-beam lithography, exposure of the photoresist in small holes is weaker than that in larger areas, while regions beyond the edges of both get some exposure from electrons scattered within the resist and reflected from the substrate. Development in large areas proceeds more rapidly because of the larger exposure. If development continues long enough to reach the bottoms of small holes, then the large areas become enlarged. The bias exposure increases the total exposure inside small holes while minimizing exposure differences caused by proximity effects.

Tetsuyoshi Ishii and his coworkers in the Patterning Technology Section at the Atsugi ECL have succeeded in suppressing resolution degradation caused by the proximity effect and by the beam-edge effect—the lack of a clearly defined edge to an electron beam. Pattern transfer is limited to a shallow region of a thick resist. This technique, which they call SIEL (superficial image emphasis lithography), has achieved patterns with 0.2-μm features separated by 0.2-μm spaces.

The resist is underexposed with an electron beam and developed to produce a concave pattern in its superficial layer. Concave patterns in the resist are planarized with a mask material that has high resistance to the resist etchant. Then the mask material is etched to the half depth of the concave patterns using a reactive ion-etch process with carbon tetrafluoride gas to fabricate a mask over the resist. A second reactive ion-etch process with oxygen gas is used to transfer the mask pattern to the resist to expose areas on the substrate that are the same size as the beam. □



Bleached. In its i-line lithography, Matsushita lays down a water-soluble contrast-enhancement layer that is bleached where struck by light. The enhancement layer cannot intermix with the resist layer.

EUROPEANS TRY TO TRADE HIGH TECH FOR SOVIET NATURAL GAS

by Robert T. Gallagher

RESTRICTIONS FROM BOTH THE EAST AND WEST COULD BOLLIX PLANS BY FRANCE AND ITALY TO CLOSE TRADE GAP

Paris

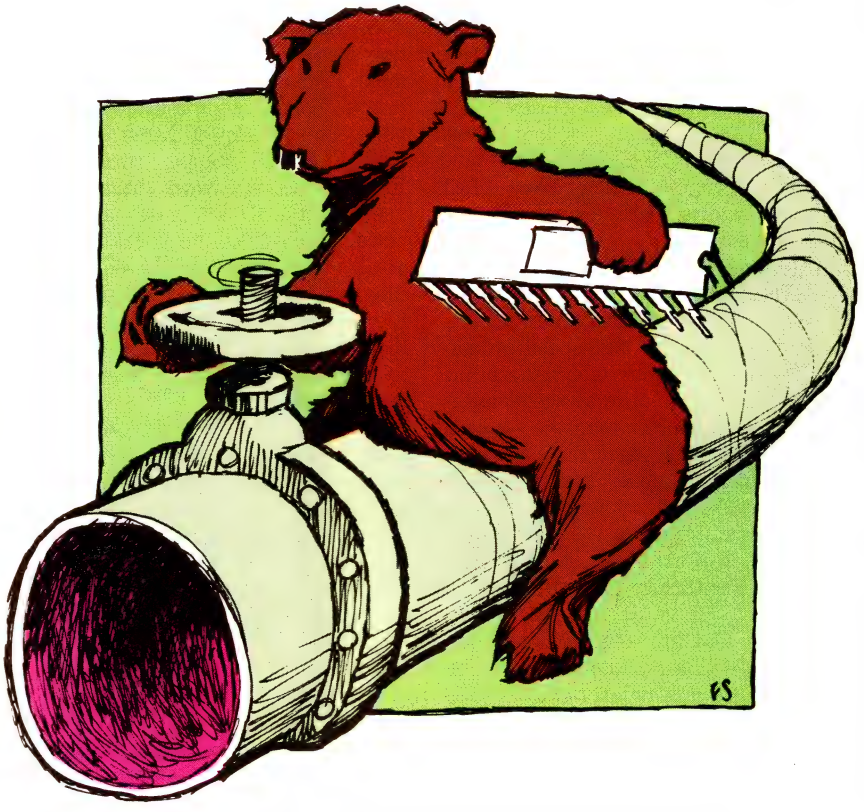
The governments of France and Italy, faced with a combined trade deficit approaching $1 billion and determined to stop paying it off in hard cash, want to make state-of-the-art technology the coin of the realm. Sales of high tech to the USSR could be the currency in their massive purchases of Soviet natural gas.

But the electronics industries of France and Italy could find the route to the Soviet market loaded with roadblocks. Some obstacles come from the U.S. and its allies, whose comprehensive export restrictions severely limit what these companies can sell to the Soviets. Others come from Soviet negotiators, who don't make life easy for potential suppliers.

Unwilling to ante. Both the French and Italian governments have stated publicly that they will not keep anteing up the cash to balance their trade deficits with the USSR. These deficits amounted to $500 million and $240 million, respectively, in 1984. Both countries have threatened to significantly cut their purchase of Soviet natural gas if the Soviets don't order more goods.

French Minister of Foreign Trade Edith Cresson said publicly that the current situation cannot continue. She also accused the Soviets of a "lack of goodwill" in their efforts to rectify the situation. Though the Soviets are paying lip service to her position by confirming that they want to "normalize" the situation through a "mutually constructive approach" to the problem, French officials are still skeptical of their sincerity.

The only recent inroad that the French have carved in the Soviet market was a contract to supply the Soviets with a toxic-gas treatment plant, thus wiping out some $250 million of the current trade gap. Because the deficit is increasing annually, though, officials in both France and Italy believe that increasing trade in a thriving industry such as electronics is the best way to eliminate the deficit in the long term.



Like most West European governments, the French and Italians must comply with strict regulations on exporting technology to Eastern-bloc countries—mostly controlling trade of products that could be used for military purposes. Though avoiding export of this equipment might seem easy, in practice, products that appear innocuous still can fall under the military umbrella.

Oversees exports. Administering these restrictions is the Cocom, or Coordinating Committee, in Paris, an informal organization consisting of representatives of all North Atlantic Treaty Organization countries, except Iceland and Spain, plus Japan. Cocom decides which technologies and equipment the Eastern-bloc countries could potentially use for military purposes. It then approves or rejects requests for licenses from companies that want to export goods that fall in those categories.

Because Cocom treats the term "military" in its broadest sense, some observers question how much electronics technology the French and Italians will be able to sell the Soviets within the organization's specifications. "I think it's a nonstarter," says one U.S. government official close to Cocom, referring to the two countries' efforts to sell electronics technology to balance their trade with the USSR. "We're talking about three-quarters of a billion dollars [total trade deficit of France and Italy with the USSR]. If they can find goods worth that much [which don't come under Cocom controls] that the Soviets are interested in having, we [Cocom] aren't doing our job very well."

Other observers aren't so sure. "We're pretty confident that they can plug quite a bit of the deficit with goods

such as computer peripherals, printers and such," says a U.S. electronics industry executive who is based in Europe. "The other thing that you have to keep in mind is that should an opportunity arise which is advantageous enough for them, they [the French and Italians] are probably not beyond interpreting the [Cocom] specifications loosely enough so that the matter can be handled domestically."

Arouses ire. Suggesting laxity toward Cocom arouses the ire of most European executives, however. "I know that some people say that we interpret the rules to our advantage," acknowledges Philippe Giscard d'Estaing, director of international affairs for Thomson SA, the giant French electronics conglomerate. "But there is absolutely no foundation to that position. We are totally scrupulous about respecting the Cocom regulations."

The real difficulty in balancing trade with the USSR. will come from the Soviets rather than from Cocom, say some observers. One snag is that the Soviets are unlikely to settle for products only. "The Soviets don't buy just equipment—they buy factories to make the equipment," points out one Italian electronics industry executive. "But even if you're ready to sell them manufacturing technology, they're still very tough to bargain with. Their negotiating approach is simple enough: they are very good at playing one potential supplier off against another."

Still, executives of nearly all major electronics firms in the two countries confirmed—most on the condition that neither they nor their companies be named—that they were negotiating technology transfer with the USSR. All point out the difficulties of transferring production capacity and technology because of the red tape in getting an export license. The transfer usually turns out to be profitable, however, because long-term sales of materials and components often follow.

Most of the companies also pointed out that they expected the trade imbalance to give them an edge over competitors from other countries. They reason that since the Soviets have a trade surplus with Italy and France, the Soviets can look at buying technology as a gas-for-technology swap, rather than a hard-cash purchase.

Still, Italtel Società Italiana Telecomunicazioni SpA is negotiating transfers of thick-film technologies for hybrid circuits and manufacturing techniques for printed-circuit boards and France's Thomson is discussing several technological transfers, mostly in consumer electronics. Thomson considers the Soviet Union to be one of its principal export target markets. □

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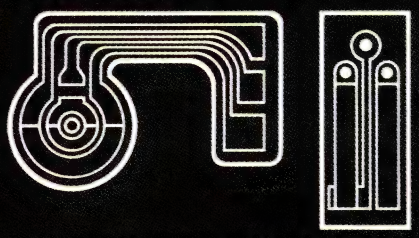

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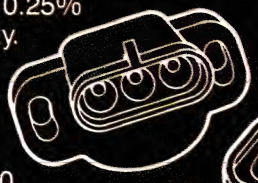

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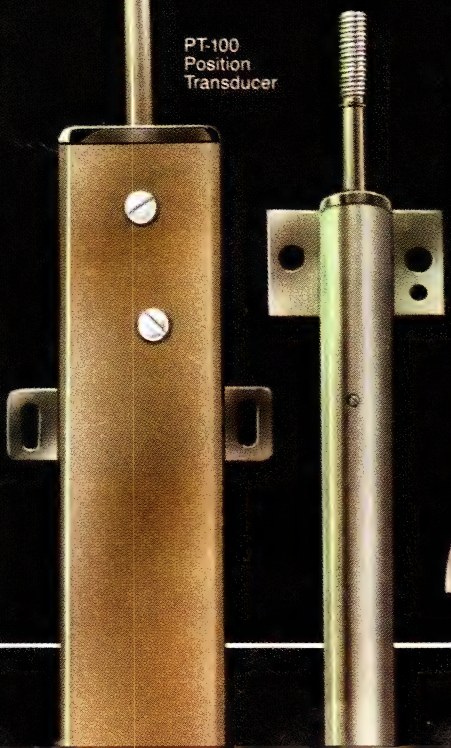

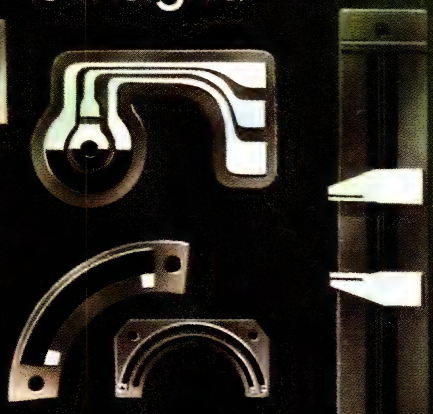

Slideline Potentiometer

CIRCLE 43

CMA CUTS RED INK ON BOOTSTRAP BUDGET

Focusing mainly on standard cells, the California chip developer goes after military market

Milpitas, Calif.

Custom MOS Arrays Inc. may soon find out how far a chip developer can progress on a limited budget. On an investment of $5 million and operating with a lean crew of 30, the three-year-old company is making its mark designing CMOS gate arrays, standard cells, and full-custom chips for the application-specific integrated-circuit (ASIC) market.

Through its Japanese production partner, Ricoh Co., CMA has shipped well over 300,000 units. Handel H. Jones, one of the company's founders and president for the past two years, says his firm is now "right on the borderline of being profitable. Our cash flow has been positive the last few months."

Hands on. Custom MOS Arrays is "on the borderline of being profitable," says president Handel H. Jones.

It is time for the privately held company to grow. "We are working on second-round financing now, looking at $4 million in equity," Jones says. He expects it to be completed within three to six months.

"He could use [the new funding] now," notes industry analyst Mary Wu of Gnostic Concepts Inc., a market research firm in San Mateo, Calif., citing the company's lean operations.

Looking at CMA's mission in the world, Jones says that "The main focus of our business is standard cells." The primary reason for this, he says, is "there is a significant weakness among the suppliers" because they concentrate on just one technology.

He admires the highly computerized efficiency of some gate-array houses (he is full of praise for LSI Logic Corp., for example) and acknowledges the silicon-efficiency advantage of some full-custom experts. However, he thinks CMA is well situated to garner a piece of the ASIC standard-cell market because of its combination gate-array and standard-cell library.

The company is nibbling at a growing market. Market research firm Integrated Circuit Engineering Corp., Scottsdale, Ariz., estimates that standard cells accounted for $90 million, or about 6%, of the nonstandard IC market in 1984. By 1990, ICE expects standard cells to grow to $2.5 billion and represent a full third of the nonstandard IC market.

Such growth has not gone unnoticed by larger commodity-chip makers, something that Jones realizes. "Everyone is looking at the profitable niches, and ASIC is considered a niche now," he says. "With the size of the business, they're smart enough to get a part of it."

Wu points out that larger companies such as Intel and Advanced Micro Devices want to foster more ASIC programs. But she concludes that with the amount of hand-holding required by that market, "there's a piece of pie for everyone."

Adds Jones: "The interface between the customer and supplier is the key deciding factor in whether you get the business. In the ASIC marketplace, you have to build relationships—that's going to make it hard for National Semiconductor and Fairchild and Signetics to get into it," because these larger companies may not have the patience to hold their customers' hands.

Sales tripled. As proof of CMA's strong track record, he points out that "we've booked 63% of the quotes we've sent out." He also says that sales for the fiscal year ending last month are triple last year's, equaling more than $150,000 per employee. This puts its sales at about $4.5 million, though the company won't disclose actual numbers.

The company's image is closely associated with Jones, a hands-on manager who often relies on personal contacts forged during his days at Gnostic Concepts (he was executive vice president from 1978 to 1981) and at Rockwell International Corp. in Dallas, where he was in charge of commercial electronics operations, including avionics and military electronics.

Using Jones's contacts, CMA is bidding for a piece of the military business, in which it already has a good portion of its design work. "In dealing with the military, you need a good track record and personal contacts," he says. "The fact that I was at Rockwell is significant for the military [as is] the fact we're willing to not require a production commitment."

Military contracts are also very smart business, Jones says, because they stimulate activity in leading-edge technology. He says that CMA is working on an agreement with a U.S. company involved in the Department of Defense's Very High-Speed Integrated Circuits program. The deal would call for trading his firm's gate-array technology for 1.25-μm processing capability.

As a selling point, CMA touts its new design capability of converting gate-array circuit designs to standard cells. Combining the two design methods into a compatible library lets customers take advantage of the low entry cost and quick turnaround time of designing a circuit in gate arrays. If it proves successful, the customer can economically convert the design to a standard cell with that methodology's smaller silicon size and lower production costs.

CMA's first conversion was done on a customer's telecommunications chip design. The 3,000-gate circuit with on-board random-access memory was first in production at the end of last year using the gate-array design. The initial production cost was over $40 a chip.

Low-cost effort. In February, the design's conversion to a standard-cell implementation was completed, resulting in a chip 20% the size of the gate-array version and costing about $5.50 each in production. Henri De Roule, vice president of sales and marketing, admits that results this dramatic are not the norm in conversions, but were achieved because of the overall gate count and threefold savings in gates by converting RAM from gate arrays to standard cells.

A more typical case involved a disk-drive-controller chip with 1,000-gate complexity. Conversion saved 30% in silicon and 25% in production costs.

CMA's customers also benefit by lowering their investment risk in a design. De Roule says the cost of a 1,600-gate-level design in gate arrays is about $25,000; converting the design to standard cells would cost an extra $30,000. Because the cost to do the design directly using standard cells would be about $50,000, the customer initially risks half as much on the design and only pays

$5,000 more for the final standard-cell version, assuming the chip goes into volume production.

De Roule, who says many of CMA's 60 customers use the dual library, notes that other companies have also evolved compatible libraries. For example, General Electric Co.'s Custom Integrated Circuit Department, Research Triangle Park, N.C., offers full compatibility between its CMOS standard-cell and gate-array libraries. *–Eve Bennett*

FOILED IN U.S. BID, SG2 STAYS ABROAD

Paris

France's second-largest data-processing and consulting firm, having shown impressive growth at home and in a long list of foreign markets, has long looked across the Atlantic at the next logical place for its expansion. The snag is that for SG2 the U.S. market is off-limits, and is likely to remain so.

Optimist. SG2 sales will double by the end of the decade, says Jean-Louis Moineau.

Ironically, the French company had a firm foothold in the U.S. little more than two years ago, with a majority share in Information Management International, a San Jose, Calif., company that provides data-processing services and systems to selected markets. That was before the U.S. Justice Department decided that SG2 was a bank and applied a regulation that prohibits banking institutions from operating other businesses. This forced the company to reduce its holding in IMI to a meager 4%.

SG2 fought the decision vigorously on the grounds that simply because its founder and principal shareholder, Société Générale, is one of France's largest banks doesn't make the subsidiary a bank. But the argument was to no avail. "This ruling is very unfavorable for us, and we are making a continuing effort to change it," asserts Jean-Louis Moineau, president of SG2. The company has engaged a U.S. law firm to try to find a way around, or through, the impasse.

Good gains. Until then, SG2 will have to be content to increase its business outside the U.S. In 1984, the company's sales reached some $160 million, an increase of 13% over the previous year. Moineau calls this growth modest compared with that of previous years, but wholly acceptable given the weak European economic climate during the period.

A net profit of just over $1 million reflects the fact that 1984 was a "year of consolidation" during which the company carried out a heavy investment program, he says. Moineau projects sales of well over $200 million in 1986, with the 1985 figures somewhere between 1984's $160 million and the $200 million goal. By the end of the decade, sales should double, to $320 million, says Moineau.

The fruits of the SG2 investment program are quite tangible. Last year, the company purchased Ordina SA, another French data-processing and consulting company, with sales of its own in excess of $10 million.

Besides broadening SG2's French activities, the merger will give the company a foot in the Netherlands market, where Ordina has a substantial subsidiary. The French company has its own foreign subsidiaries—six on the Continent, five in Africa, one in Brazil, and two to serve the Far East.

New blood. Besides buying a company last year, SG2 founded one. SG2TEL will use computers from Prime Computer Inc. to serve telematics—the overlap of data processing, office automation, and telecommunications services—and videotex customers from its headquarters in the Paris suburbs. SG2 already serves more than 10,000 videotex clients from eight French regional centers.

Besides telematics, SG2 specializes in communication networks, payment systems, and production automation. It is one of the principal French companies dealing in the connection of heterogeneous data-processing equipment, which it carries out for industrial and governmental clients.

The firm's research and development program will get a shot in the arm in the coming years from participation in three of the European Communities' Esprit projects—one each in information-exchange systems, wideband networks, and communication systems and architectures. *–Robert T. Gallagher*

BOTTOM LINES

COMPANIES STILL SEEK SENIOR EXECUTIVES

The good news is that demand for senior executives in U.S. corporations is as strong now as a year ago, and 35% ahead of demand in June 1983, according to a survey by Lamalie Associates Inc., an executive search firm in New York. But the bad news is that demand for middle managers has eroded deeply.

"Companies will continue to seek talented senior executives to lead their operations during the second half of 1985," said company chairman Robert E. Lamalie. But the outlook for middle managers remains bleak as firms take more steps to cut costs and streamline operations, he says. "The relatively lean middle-management ranks will probably absorb further shocks this year."

Lamalie cited competition among high-technology companies, especially computer and semiconductor firms, to explain why companies are looking for senior managers. "The long-anticipated shakeout in high-technology companies is here, and some simply will not survive the year," he said. "The leading firms are seeking executive leadership that can reposition their businesses favorably against domestic and international competition."

INDUSTRY MERGERS DROP 17% IN 1984

Electronics-industry mergers and acquisitions dropped 17% last year from 1983, according to W. T. Grimm & Co., a Chicago consulting company. Grimm's latest statistics show that mergers and acquisitions in the electronics industry in 1984 totaled 67, compared with 81 in 1983. So the electronics industry ranks 13th on Grimm's 50-industry list of mergers and acquisitions. The dollar value of the acquisitions in the electronics industry totaled $290.1 million last year, down from 1983's $471.9 million.

EMHART ACQUIRES EUROPEAN COMPANY

Emhart Corp., Farmington, Conn., whose Electrical/Electronic Group makes and sells capacitors in the U.S., has purchased the Arcotronics Group, a European producer of capacitors, to boost its capacitor sales in Europe. Emhart bought Arcotronics from Wedge International Holdings BV, London, for $61 million—$53 million in cash and $8 million in assumed debt. Arcotronics, which employs 1,600 at facilities in Italy, West Germany, the UK, and the U.S., manufactures a line of metallized plastic-film capacitors.

PIONEER KAO GOES AFTER OPTICAL PROCESSOR AT ITT

London

It's been almost 20 years since Charles Kao, together with George Hockham, published the historic paper that outlined a revolutionary system of communication by transmitting light pulses through optical fibers.

Still on top. Fiber-optics pioneer Kao is ITT's executive scientist.

Kao, then a researcher at Standard Telecommunication Laboratories in Harlow, England, did not just invent a technology. He turned it into a practical system, collecting over 29 basic patents along the way.

Kao's 1966 achievement might have jaded the curiosity of many researchers. But Kao, who looks far younger than his 52 years, confesses, "My enthusiasm is still increasing rather than diminishing." To honor his accomplishments, the Institute of Electrical and Electronics Engineers last month awarded Kao the Alexander Graham Bell Medal for "pioneering contributions to optical fiber communications."

Today he is still at the leading edge of optoelectronic research. In 1982, Kao was named ITT Corp.'s first executive scientist. ITT created the position to let him return to research in any subject of his choice. He chose very high-bit-rate communications and signal-processing systems that operate at rates of trillions of bits per second.

Kao is now tackling the problem of matching a fiber's huge optical bandwidth to the terminal equipment it is connected to. He is looking into the feasibility of all-optical communication, switching, and processing systems.

Reserved reponse. As for optical processing, he says, "It cannot do everything, it can only do some things well. For one thing, optical systems are naturally parallel in operation." Kao won't say more, reserving the results of two years thinking on the topic for an IEEE publication marking optical fiber's 20th anniversary.

Kao reflects that the pace of research has changed in recent years, and breakthroughs by a single researcher or research team are becoming less likely to happen. "Long-term research must be cooperative research. This is because the scale of the research effort and the resources available are beyond any one group. Besides, a single group has too narrow a view of the problem."

Kao has become a nomad, constantly moving among the three laboratories within the ITT group and 10 universities he is working with. He remains in close contact with the European Joint Optical Bistability (EJOB) project, a program funded by the European Community that aims to demonstrate an optical computer.

Kao is now working with ITT's subsidiary in West Germany, Standard Elektrik Lorenz AG, on the installation and trial of a wideband, fiber-optic network to provide homes and businesses in Stuttgart with communications, business, and information services. An integrated-services data network, says Kao, is possible only with fiber optics. *–Kevin Smith*

A FEMALE TEAM DESIGNS A SONY TV

Tokyo

I don't want recognition as a woman. I just want the chance to contribute my talents," says Sony Corp. product planner Keiko Watanabe. She and the three other women on her design team got that chance. The result—a high-fashion TV set—is the first Japanese consumer-electronics product designed and marketed by an all-female team.

"It really wasn't planned that way, even though we have attracted a lot of attention," says the 29-year-old Watanabe, who has a bachelor's degree in sociology and has been at Sony for seven years. She was promoted recently to assitant planner in the Consumer Products Assistant Group.

Teamwork. Keiko Watanabe (second from left) headed Sony's all-female design team.

"Inside the company, there is a trend toward giving women more influence in product planning and design," Watanabe says, though male Sony engineers did the technical work. She supervised market research and product development. Kazue Kato was responsible for cabinet design and color, Yukiko Okura for logo design, and Rumi Nakano for packaging design.

The TV set they produced, C'est Pia, comes in a choice of colors—including pastel pink. Its target is the young adult market. "The goal was to design a more compact set, with a smaller screen than conventional 12- to 14-in. models," says Watanabe. To suit the tastes of young Japanese, she says the team also wanted to "design a set that could be an interior decoration item as well as an entertainment product."

The set has a 9-in. screen and a control that allows the viewer to convert the picture from a conventional color display to a single color in a range of hues, including sepia. The color-adjustment control also can turn the set into a background lamp.

Measuring 8.8 by 9 by 12.5 in., C'est Pia sells for $299, which includes a remote control. Marketing in Japan began in late May, with a monthly sales goal of 5,000 sets.

Male resistance. Team members say the project's major difficulty wasn't the 18 months of planning but male colleagues' skepticism, even after the team had positive test-marketing results. "We wondered how they could be so sure we were wrong, when they didn't even know much about the latest fashion trends," Watanabe said.

"Most Japanese men simply regard women as gentle or tenderhearted, and they expect to see that in our work," says team member Kato. "When I made my early sketches, they kept telling me, 'This doesn't represent the work of a woman.' We had to convince them we weren't designing a feminine product, but one that could appeal to young men or women."

Yet logo designer Okura says the cabinet's subtle hues and the idea of using the screen as background lighting are characteristic of a feminine approach. "Women consumers always have had male-dominated products imposed on them," says Watanabe. "Now we're starting a new era." *–Michael Berger*

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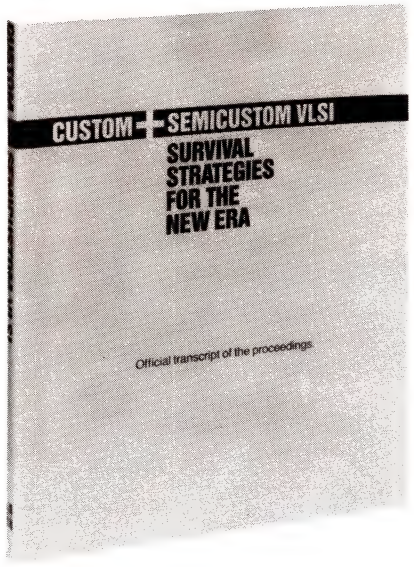

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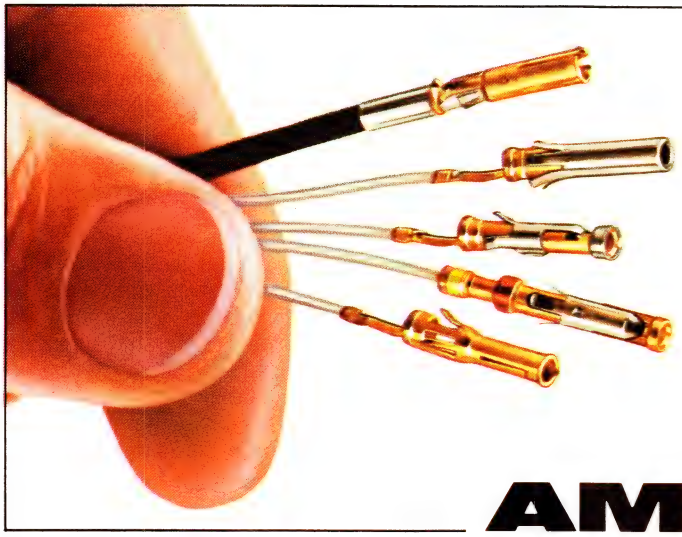

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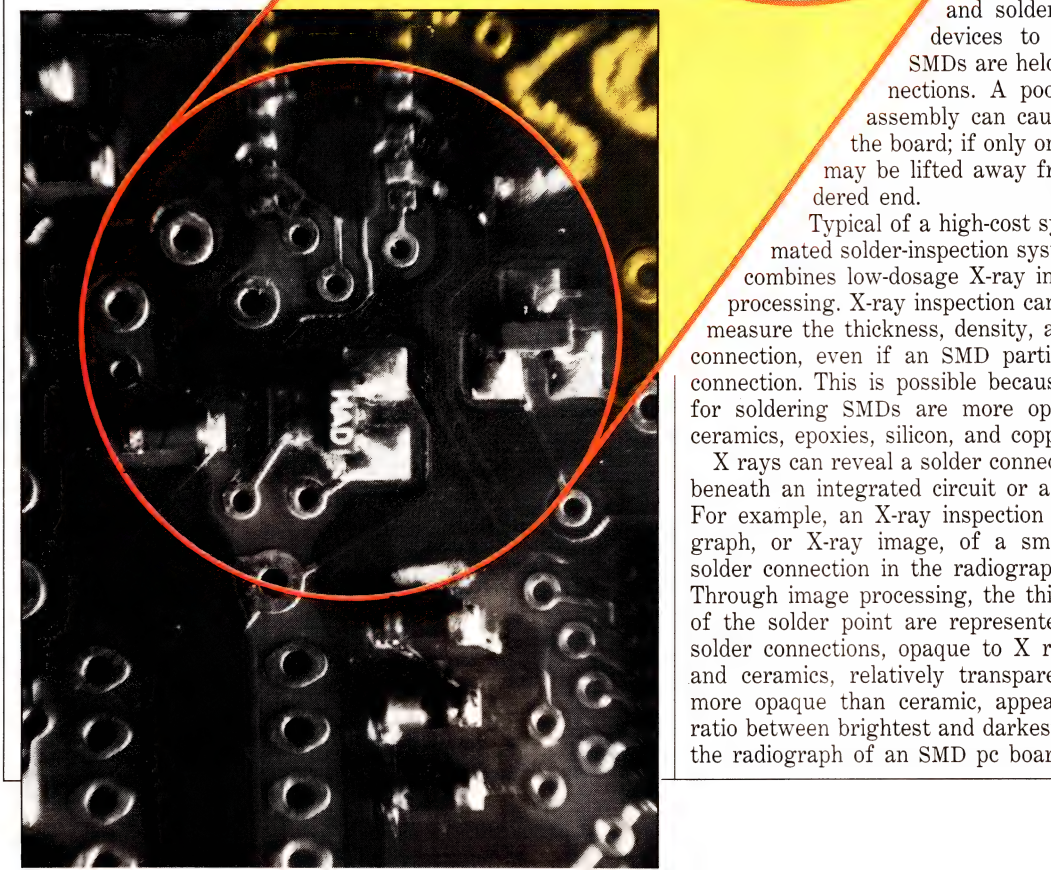
PACKAGING CHANGES MAKE AUTOMATIC TESTING TOUGHER, MORE COSTLY

by Howard Bierman

THE SHIFT TO SURFACE-MOUNTED DEVICES AND INCREASED SENSITIVITY TO LINE NOISE PLAGUE TEST ENGINEERS

Installing automatic test equipment on the factory floor has always been a difficult, expensive job. But in today's electronic equipment designs, the problem of testing is getting even tougher and more costly because of the significant changes now going on in component packaging. The quickening trend toward tiny, leadless surface-mounted devices, for example, makes accessibility to soldered connections on circuit boards more difficult. In addition, both the products to be tested and the automatic testers are becoming increasingly sensitive to the noisy environment of the factory floor.

Faced by the rapidly escalating costs of testing on the production line, managers and test engineers are looking harder than ever for lower-cost ways to do the job. They are improvising alternatives to multiple stations of very large-scale-integration or functional board testers, which can cost as much as $1 million each. One approach is to mix and match a low-cost in-circuit analyzer or a short-circuit tester with a functional board tester as a prescreening process. This already has effectively raised test throughput at dramatically lower costs.



1. Solder-joint radiographs. Inspection of SMD-loaded pc boards by X-ray imaging is effective because metallic alloys used in solder are opaque to X rays, copper is less opaque, and ceramics and epoxies are transparent.

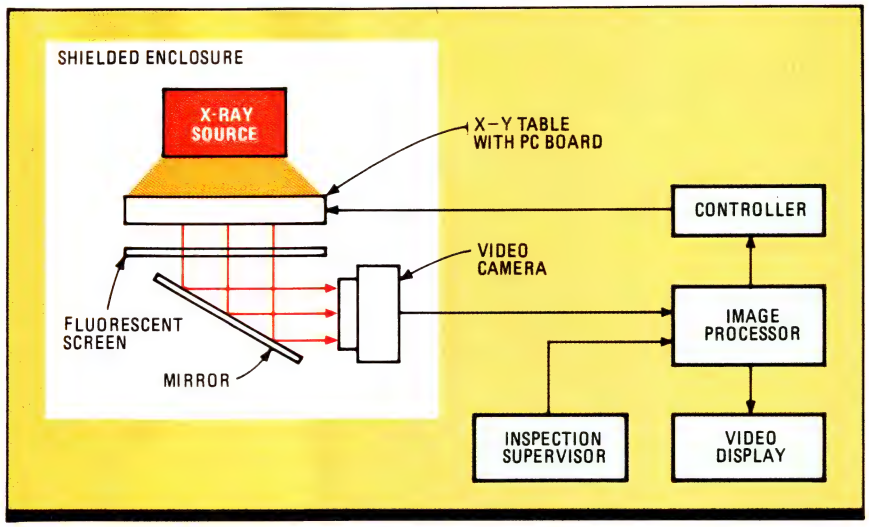
The proliferation of surface-mounted devices causes a lot of problems for test engineers. Because of their small size and the location of solder connections underneath the package, SMDs make the testing of solder connections a challenge in the manufacturing process.

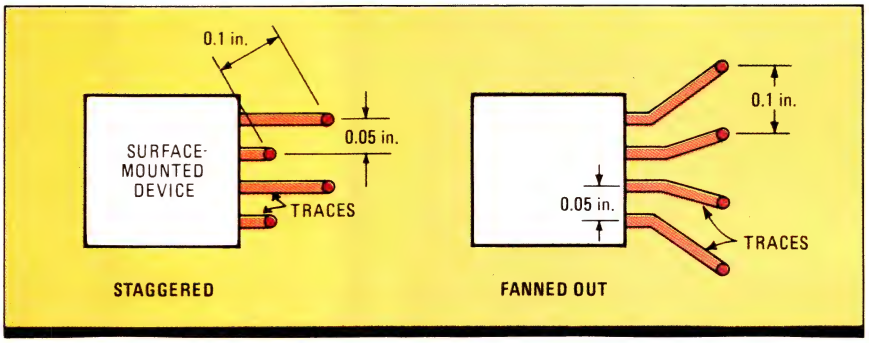
"While SMDs are used in fewer than 10% of circuit boards today, their growing acceptance will increase to nearly 50% within the next five years," says Mike Juha, marketing manager of IRT Corp., San Diego. Through-holes and solder hold conventional leaded devices to the printed-circuit board; SMDs are held solely by their solder connections. A poor solder joint in an SMD assembly can cause a component to fall off the board; if only one end is soldered, the SMD may be lifted away from the board at its unsoldered end.

Typical of a high-cost system, the company's automated solder-inspection system for SMD-loaded boards combines low-dosage X-ray imaging and computer-aided processing. X-ray inspection can accurately and repeatedly measure the thickness, density, and shape of a good solder connection, even if an SMD partially or fully obscures the connection. This is possible because the metallic alloys used for soldering SMDs are more opaque to X rays than the ceramics, epoxies, silicon, and copper used for pc boards.

X rays can reveal a solder connection even when it is buried beneath an integrated circuit or a multilayer circuit pattern. For example, an X-ray inspection system can make a radiograph, or X-ray image, of a small-outline transistor; each solder connection in the radiograph appears as a dark area. Through image processing, the thickness, density, and shape of the solder point are represented in shades of gray. The solder connections, opaque to X rays, appear black; epoxies and ceramics, relatively transparent, appear white; copper, more opaque than ceramic, appears gray. Close to a 100:1 ratio between brightest and darkest areas can be displayed on the radiograph of an SMD pc board (Fig. 1).

2. X-ray inspection setup. The fluorescent screen changes the radiograph to a visible image so it can be scanned, when reflected by the surface mirror, by the video camera. The image processor converts analog output from the video camera into digital form.





3. Staggered test pads. So that relatively low-cost 0.10-in. center probes rather than delicate 0.05-in. ones can be used, test pads on SMD assemblies should be staggered or fanned out.

In the IRT X-ray inspection system, a shielded enclosure contains the source for generating X rays in the 160-KeV range. The system directs the X-ray beam upward toward the circuit board and creates an image, based on the density and thickness of the assembled elements, on a fluorescent screen to convert it into a visible-light image. A high-resolution video camera captures this image. A surface mirror keeps the harmful X-ray beam away from the video camera (Fig. 2).

The system feeds the analog signal produced by the video camera out of the shielded enclosure for digitization by the image processor to determine the size, thickness, and density of each solder connection. Microprocessors enhance and analyze the image in about 0.033 s to allow viewing on the system's display.

The inspection supervisor console permits the user to start, stop, and select a part through a touch-screen menu. The system provides a library of inspection routines for SMDs and dual in-line packages to help the user develop necessary inspection procedures. After trial inspection of several pc boards, the user can develop inspection criteria with large measurement deviations, making it easy to separate the good boards from the bad.

Although the equipment costs more than $400,000, the typical payback period "is less than one year, with savings stemming from reduced inspection labor, improved product yield, and higher assurance of pc-board quality," Juha claims. With this type of automated inspection, typically less than one board per 10,000 inspected will be falsely accepted as good, and less than one board per 1,000 inspected will be falsely rejected as bad.

Test pads a must for SMDs

Wave and reflow soldering are the two common methods of making electrical and mechanical contact between SMDs and pc-board traces. Because of the close centers between SMD leads and traces (0.10 in. and closer), shorts are a common problem, especially with wave soldering. Solder-ball shorts are prevalent with reflow soldering. Other production problems that plague SMD-loaded pc boards include missing components, parts of incorrect value, and misoriented ICs.

Missing components are not unusual in SMD assemblies—only the solder holds a device in position. In wave- and reflow-soldering, insufficient adhesive or solder paste will allow an SMD component to become dislodged. Because many SMDs are unmarked, components of incorrect value can become a problem on the production line. Incoming inspection stations and in-line process control minimize this risk. Misorientation of parts—ICs, for example—also creates serious problems.

Testing pc boards loaded with tightly packed SMDs is no easy task, because SMDs cover many of the solder joints and circuit nodes. Unlike conventional leaded pc boards, which permit probes to examine test pads on the reverse side of the pc board, SMD assemblies must be designed from the beginning with testability in mind. Probing SMD boards is especially difficult when parts are spaced on centers as close as 0.07 in., which requires delicate 0.05-in. probes. These probes have a slightly higher resistance than the standard 0.10-in. center probes, and they tend not to last as long.

Many newer assemblies mix SMDs with leaded components on both sides of a pc board, further aggravating the test engineer's problems. Two-sided in-circuit test fixtures, or clamshells, though feasible, are expensive and require considerable time to build.

The force of a 4- or 8-oz sharp-tipped probe on the top or side of an SMD could ruin it. In addition, probe pressure on a poor or open solder joint can force contact and thus allow a defective board to be passed. Excessive mechanical pressure, with possible board damage, can result if too many probe points are concentrated in one small area; the total force of all probes could crack a ceramic SMD package or damage a solder joint. For fragile pc boards, a mechanical fixture might be more appropriate than a vacuum fixture.

It is good practice for pc-board designers to include test pads along the board trace. It is also good practice to position test pads on 0.10-in. centers so that conventional rather than custom bareboard testers can be used. If the board includes tall components or heat sinks, the test pads must be located at least 0.20 in. away to give the probes enough room to make proper contact. Solder should cover test pads to provide good contact for the test probes. Vias can be used as test pads, but the holes should be filled with solder to prevent the probe from getting stuck.

Flatpacks, chip carriers, and small-outline ICs come in a variety of sizes, with lead spacing of 0.05 in. or smaller. To avoid compounding the probing problem, test pads should be staggered or fanned out (Fig. 3).

As manufacturers strive to increase production, the question becomes not whether to use ATE, but how much to spend

on it. Because of the rapid drops in price for computers, memories, and peripherals, today's low-cost ATE (under $100,000) equals or exceeds the performance of the high-cost ATE designed several years ago [*ElectronicsWeek*, March 25, 1985, p. 61].

The tradeoffs for low-cost ATE are predictable: less test comprehensiveness, slower test and diagnostic speed, and limited data logging and analysis. When the goal is a state-of-the-art product, high-cost ATE is preferred. For automated factory production, manufacturers must consider many factors: production volume, product complexity and mix, availability of skilled technicians, response time to deploy a test system, development time for test software, and availability of money.

One question is whether the manufacturer can use the same ATE system not only for production testing but also for service and repair to reduce the high cost of maintaining a board inventory in the field. Another is whether assembly and process-induced faults represent a significant percentage of production defects on a particular board design rather than out-of-tolerance passive components or semiconductors. Such questions must be faced before making the profound decision on how to mix and match loaded-board shorts testers, in-circuit analyzers, in-circuit testers, and functional board testers, says John Bateson, marketing manager of Factron/Schlumberger, Titusville, Fla.

In-circuit testers power the assembled pc board and check for opens, shorts, correct component placement, orientation, and parameter values. The assumption with an in-circuit tester is that a properly assembled board with good parts results in a good board. Functional board testers, by contrast, exercise the board's performance and make a go or no-go decision. In-circuit testers range from $75,000 to hundreds of thousands of dollars; functional testers range from slightly under $100,000 to $1 million. Furthermore, software-development costs for ATE generally equal and often considerably exceed the hardware cost, Bateson says. Therefore, the testing cost per board, regardless of volume, is significant. Any means that directs some of the test burden from expensive ATE to a lower-cost alternative can result in substantial savings.

As board manufacturers realize where the greater profits lie, they are shifting their emphasis from defect location and removal to defect prevention. For this reason, a recent study by Logical Solutions Inc., Campbell, Calif., indicates that functional board testers that check overall assembly functions will increase their market share from 40% to 60% over in-circuit testers by 1988. In-circuit testers detect board defects and pinpoint which components to replace.

Board testing can be performed with low-cost loaded-board shorts testers and in-circuit analyzers as well as with expensive in-circuit and functional board testers. A loaded-board shorts tester takes between two and six hours to program and finds shorts quickly; its effective fault coverage falls between 35% and 65% (Fig. 4). In-circuit analyzers cover between 50% and 92% of the faults; programming takes from one to four days. An in-circuit tester offers 85% to 96% fault coverage, but fixture-design time may be extensive and programming can take longer than six weeks. A high-capacity functional board tester screens out about 98% of the defects but could take nine months to program.

One-to-one cost comparisons

If shorts are a major source of faults, a low-cost ($20,000) loaded-board shorts tester in tandem with an in-circuit tester will increase product throughput and allow more time for the more complex testing requirements the in-circuit tester can handle. Functional testers, which are highly inefficient for diagnostics, achieve a dramatic increase in product throughput when used with a loaded-board shorts tester to handle the shorts-testing task.

The advantages of a low-cost loaded-board shorts tester include low cost of testing (typically less than $1 per pc board), fault detection (typically less than $2 per pc board),

FACTORY ATE: TO LEASE OR NOT TO LEASE?

"Engineering managers face tough odds to get approval for their test-equipment budget as corporate managers and their financial advisers seek to reduce capital expenditures in 1986," warns Edward Herman, president of Equitable Life Leasing Corp., San Diego. Though nearly 70% of the Fortune 1,000 companies lease capital equipment, many small and inexperienced firms do not: its tax advantages are meaningless when profits are low. However, electronics firms can benefit in many ways by leasing, says Herman, especially if they intend to use the equipment for two years or less.

There are two popular forms of leasing: direct finance capital leases, which require that the lease be capitalized on the lessee's balance sheet, and operating leases, which do not appear on the lessee's balance sheet. Many companies evaluate their subsidiaries or divisions by return on investment, which makes operating leases attractive because the asset is paid for in the form of rent. No stock or bond offering to gain the necessary capital is required, and a bank loan is unnecessary. Most prime contractors on government projects use operating leases to get equipment because they receive more favorable reimbursement than for outright purchase, Herman points out.

In many firms, capital equipment budgets are approved annually, with annual or semiannual reviews. This can draw out the process of ordering, acquiring, and installing test systems. Leasing, by contrast, is less stressful to the budget in that it involves only rental cost for the time the equipment is needed. Many companies are limited in their loan agreements to a specified balance-sheet ratio, thus preventing outlays for purchase of capital equipment. Again, an off-the-balance-sheet operating lease offers the means to get the necessary equipment on the test floor. Finally, as Herman notes, leasing can sidestep the trap of rapid obsolescence (and depreciation) of test equipment when faster, better testers hit the market at lower prices and newer, faster devices and systems needing more sophisticated testing go into production.

Herman recommends several steps to come to a decision: analyzing what equipment is needed, estimating the equipment's lifetime, evaluating whether it can be upgraded to handle more complex devices or systems in the future, determining the tax advantages of leasing and buying, and considering the company's financial position.

If the decision is to lease, factors such as the terms of the lease, maintenance, delivery, and training should be negotiated as thoroughly as they would be for a purchase. The lessee should determine if the leasing company carries the equipment required, can maintain the equipment or provide a rapid replacement, and is well capitalized and technically competent to advise on equipment modification and upgrading.

One word of caution is in order. Because software-development costs may become greater than even the rental cost, it is important for the lessee to negotiate a strong option-to-buy clause. **–H. B.**

fast test and diagnostic time (usually less than 10 seconds), and rapid test-program development. On the negative side, this type of tester limits fault coverage to shorts and requires a bed-of-nails test fixture (which can be expensive and take time to fabricate).

If manufacturing-induced faults and analog component defects are responsible for the majority of board failures, a relatively low-cost ($43,000) in-circuit analyzer can be used in tandem with an in-circuit tester or functional board tester to reduce testing costs and improve throughput. The in-circuit analyzer is three times faster than an in-circuit tester in detecting manufacturing-induced faults, offers test and diagnostics usually within 10 seconds each, and is relatively simple to program, says Bateson. But because it is unpowered, an in-circuit analyzer cannot test digital logic faults; either the in-circuit tester or functional tester following the in-circuit analyzer must locate these logic faults.

Low-cost prescreening

A low-cost loaded-board shorts tester or in-circuit analyzer can be used to prescreen an expensive in-circuit tester ($220,000) or functional board tester ($370,000). To permit a one-to-one comparison, Bateson set up a hypothetical situation involving 15,000 central-processing-unit boards undergoing testing with a first-pass yield of nearly 70%. In this example, shorts predominate: there are 3,800 defective boards with 2,808 shorts among 5,580 total faults. Because shorts are a major problem in this case, it is useful to compare short detection for a loaded-board shorts tester, an in-circuit tester, and a functional board tester (see table).

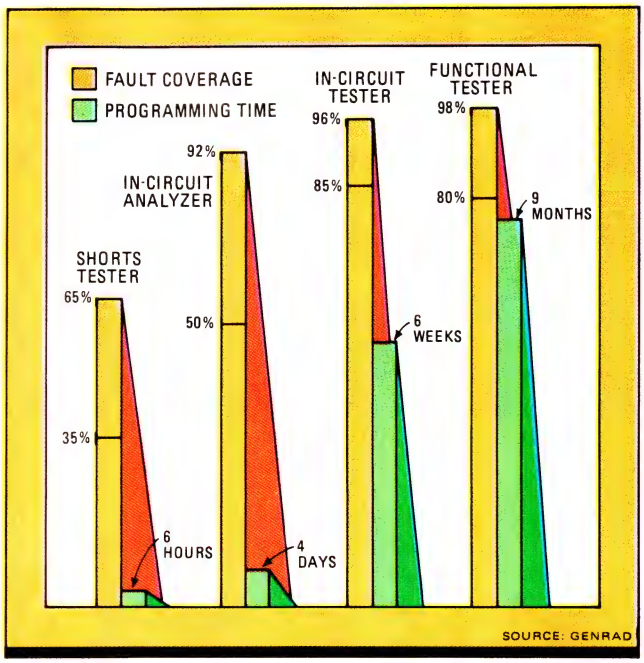
The loaded-board shorts tester is more than twice as fast as the in-circuit tester for locating shorts; the functional board tester is considerably slower. When the time needed to test all boards, good and defective, is combined with the total expense, the result is a test cost of 12¢ per board for a loaded-board shorts tester, four times that much for an in-circuit tester, and more than 10 times more for the functional board tester. Throughput is six times faster for an loaded-board shorts tester than for the functional board tester.

Placing a loaded-board shorts tester ahead of the in-circuit tester to prescreen for shorts lowers the effective test time to 124.25 hours, for a 7% increase in product throughput and an added cost of $1,089 over the in-circuit tester alone. Further improvement occurs when the shorts test is eliminated from the in-circuit tester (it is done by the loaded-board shorts tester): total test time drops to 106.75 hours, and throughput increases an additional 15%.

Combining the loaded-board shorts tester with a functional board tester produces even more dramatic results. The functional board tester alone requires three to four hours of test time for a product throughput of 0.82 boards/min. The combination of a loaded-board shorts tester and a functional board tester boosts throughput by a factor of 5.6—to 4.6 boards/min.—providing an $18,000 reduction in test expenses. It must be emphasized that these results apply in situations where board shorts are the dominant type of failure.

Consider the same 15,000 CPU boards with not only the identical shorts defects but also 2,340 assembly-induced faults on 84 pc boards. An in-circuit analyzer can be used to locate and diagnose shorts and component faults, and its performance can be compared with an in-circuit tester and functional board tester. The low-cost in-circuit analyzer requires 80 hours for test, while the higher-priced in-circuit tester and functional board tester need 150 and 490 hours, respectively. Combining an in-circuit analyzer with an in-circuit tester drops test time to 124.25 hours or two pc boards/h, a 21% increase in throughput for a modest $1,200 additional expense.

By eliminating the redundant manufacturing-induced faults test that both the in-circuit analyzer and the in-circuit tester perform and assigning this task to the in-circuit analyzer, throughput is further improved to three pc boards/min, a 50% improvement. An in-circuit analyzer used to prescreen an expensive functional board tester reduces test time from 490 hours to 80 hours, a sixfold increase in throughput that reduces test expenses by $32,000 compared with the functional board tester alone.



4. Board-tester tradeoffs. Low-cost loaded-board shorts testers take only hours and offer up to 65% fault coverage. Functional testers reach 98% fault coverage but need months of programming time.

"Both the loaded-board shorts tester and the in-circuit analyzer appear to be an ideal investment for the first-time commercial ATE user," concludes Bateson.

Tracing dirty power

The high-speed, dense electronic products and components coming off the production line today as well as the computer-automated equipment used to test them are especially susceptible to noise pulses from a variety of noise-generating factory equipment. Erroneous measurements on pass-or-fail tests could impair test throughput or, even more seriously, allow defective products to pass inspection. Semiconductor chips under test can also be damaged or destroyed as high-energy pulses or line-voltage surges stress the fine-line geometries separating individual cells.

The cause of dirty power is easy to trace, says Peter Nystrom, manager of the Central Engineering Division of Oneac Corp., Bannockburn, Ill. The power utility delivers power to the service entrance of the factory, and the power is then distributed throughout the building. As plant operation gets under way, motors and relays turn on and off, machine-shop drills and saws go into action, conveyors and part handlers begin their operation, and the power lines become infested with noise pulses ready to sabotage the computer-aided ATE installations.

The noise pulses can be in either the normal (line-to-line) mode or common (line-to-ground) mode. "Common-mode electrical noise poses a special threat to modern electronic circuitry since the safety ground line to which common-mode noise is referenced is often used as the system's logic reference point," Nystrom warns. Since parasitic capacitance exists between safety ground and the reference point, at high frequencies these points are essentially tied together, allowing noise to directly enter the system's logic.

A switch-mode power supply also produces dirty power;

PRODUCTION-LINE COSTS DEPEND ON TESTER TYPE

Parameter*	In-circuit analyzer	Loaded-board shorts tester	In-circuit tester	Functional board tester
Initial price	43,000	24,000	220,000	370,000
Fixturing	1,670	1,670	1,670	310
Programming	860	350	2,130	8,560
Total test time (hours)	80.08	57.14	132.71	304.03
Labor expense	2,082	1,486	3,450	10,337
System expense	424	167	3,594	13,724
Setup expense	115	137	257	623
Total expense	2,621	1,790	7,301	24,684
Test cost per pc board	0.17	0.12	0.49	1.65
Cost per fault	0.50	0.64	2.60	8.79
Throughput (pc boards/min)	3.12	4.38	1.88	0.82

*in dollars unless otherwise noted

unhampered by the bulky 60-Hz power transformer, the large filters, and the heavy heat sinks used by its linear-power-supply predecessor, the switch-mode design (which operates at up to 50 kHz) is more efficient and comes in a smaller and lighter package. Unfortunately, the supply is also loaded with potentially damaging pulses because of its high crest factor. Crest factor, defined as the ratio between peak current and root-mean-square current, is 1.414 with a resistive load but can rise to 3 or greater with nonlinear loads such as switch-mode power supplies.

Comparing two loads—one resistive and one a power-supply load—that both require 10 A rms, the resistive load is sinusoidal and demands 14 A per half cycle; the switch-mode supply requires 30 A every half cycle, and current transfer is four times faster than the resistive load. The utility can handle these load-current peaks with its low-impedance source. If the power-supply load is high-impedance, however, a quick transfer of current to the load is inhibited, forcing the power supply to extend its duty cycle and reducing its voltage regulation. In addition, the high-impedance path will create a sharp electrical noise pulse as a result of inductive kickback.

Getting to the root of the problem

When production-line process deviations crop up and if the problem is in the power lines, the next step is to determine its seriousness, duration, frequency, effect on measurements, and repair cost. Testing the wiring usually means monitoring the building lines and the quality of the incoming power for at least a week. Power problems caused by utility companies include surges, sags, brownouts, interruptions, and blackouts.

Tools for cleaning up power run the gamut from inexpensive transient suppressors to sophisticated power conditioners. Transient suppressors cannot cope with sags or excessive over- and undervoltages. Furthermore, if a transient suppressor is connected between line and neutral in the power-distribution system, noise impulses may be diverted into the system ground where they will cause more harm than good.

Another inexpensive fix is an isolation transformer, but unfortunately this offers poor normal-mode attenuation with no voltage regulation. An improved isolation transformer, called an ultra-isolation transformer, is built with grounded Faraday shields to reduce interwinding capacitance. So it reduces noise coupled from the transformer's input to its output. But normal-mode isolation is not provided because noise transients occur too rapidly to saturate the transformer.

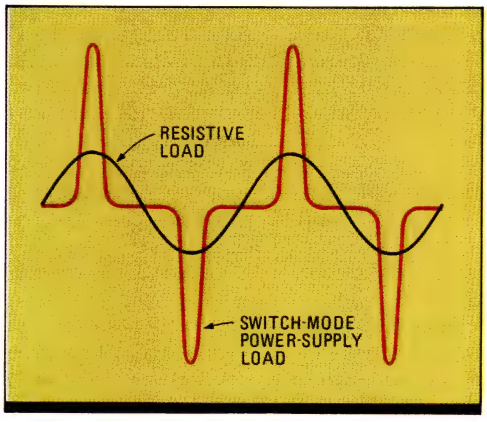
Ferroresonant transformers, operating with saturated cores created by a 60-Hz resonant tank circuit, provide good voltage regulation and isolation because the core is effective at blocking the impulse noise. However, these transformers also have drawbacks—notably a high transfer impedance that creates high-amplitude voltage spikes and relatively low efficiency (typically 75%).

A low-impedance power-line conditioner, with high normal- and common-mode rejection and high efficiency (up to 98%), offers the optimum solution. A power conditioner contains several components: a specially designed isolation transformer, radio-frequency coils, capacitors, and clipping devices, all placed in series with the ac utility line. The conditioner's function is to eliminate any transients and noise pulses and to provide a low-impedance interface between the factory equipment and the utility. According to Nystrom, an ideal power conditioner has six basic abilities:

- Isolation of normal- and common-mode noise.
- Energy transfer on demand, without resistive or inductive losses.
- Stability under all line and load conditions.
- Low output impedance to prevent the conditioner from introducing noise into the system.
- Ability to not extend or distort a line-voltage notch.
- Efficiency of greater than 96% to keep heat load down and equipment working.

There is another alternative: to simply create a source of clean power by converting the utility ac voltage to 70 V dc to power a stable oscillator delivering a low-level pure sinusoidal output, from 45 Hz to 10 kHz (Fig. 5). Such firms as Behlman Engineering Corp., Carpinteria, Calif., offer this solution.

In this method, the output of the low-distortion oscillator is fed to one, or in some cases several, linear power amplifiers. These, in turn, will deliver up to an 18-kVA single-phase or a 54-kVA three-phase output. Line regulation during the process is held to within 0.1% for 10% variation in line voltage.



5. Clean power. Converting incoming power-line ac to dc, applying it to a stable oscillator circuit, and then amplifying a pure, noiseless, sinusoidal output delivers the power levels required.

Assuming that clean power is so critical for ATE performance, why don't ATE manufacturers build noise protection into their high-priced products? Vendors say that it is because the high costs of such measures would drive ATE prices up even further and put the manufacturer at a competitive price disadvantage. And some ATE suppliers say that dirty power at the customer's site is the customer's problem, not theirs. In the final analysis, the test engineer is responsible for controlling the ATE-power interface for optimum test accuracy and yield. □

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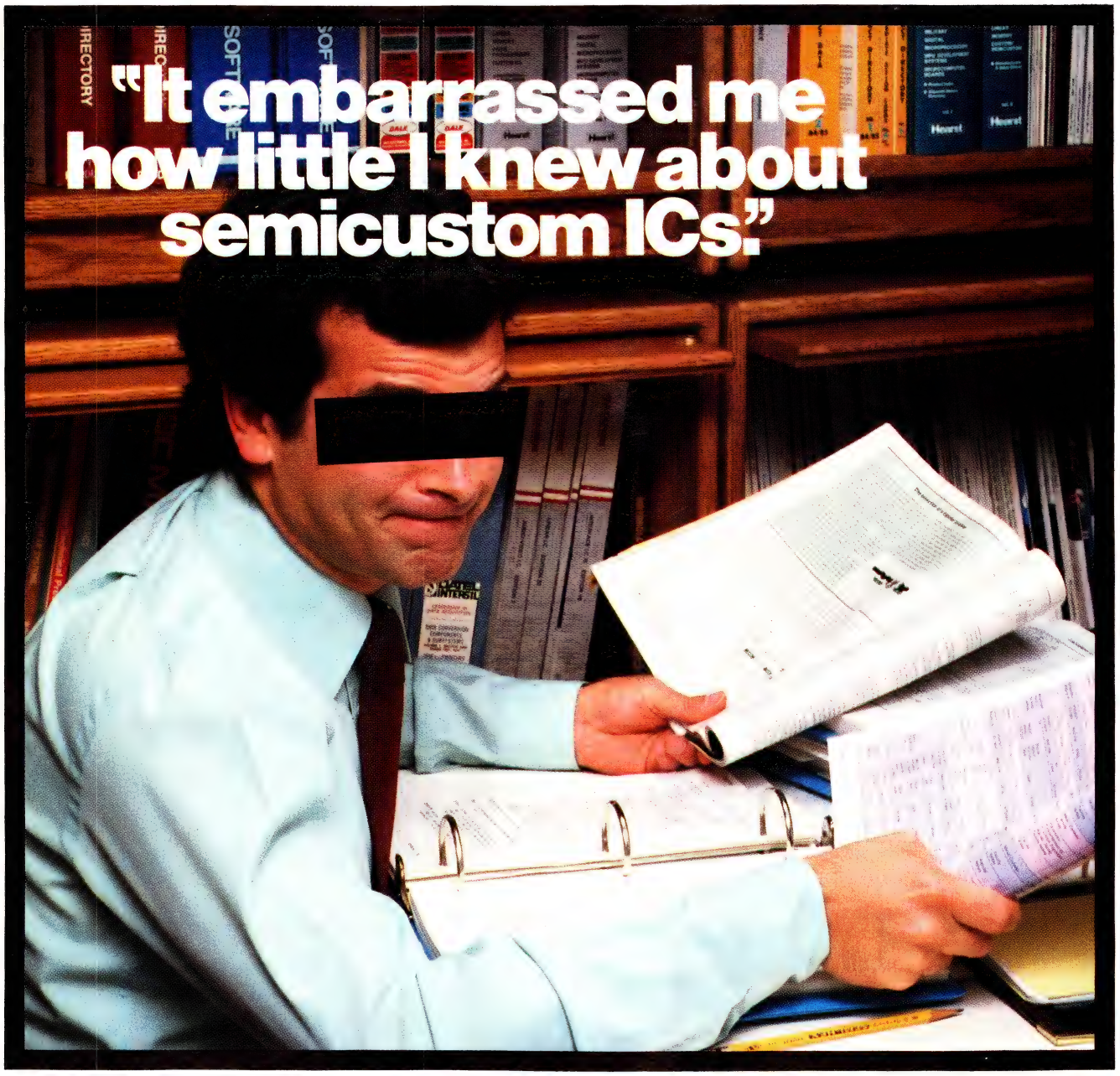

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A RISC SYSTEM THAT LIKES FLOATING POINT

Ridge's redesigned central processing unit operates up to four times faster

Reduced-instruction-set computers, a relatively new approach to computer architecture, increase computer performance while lowering cost. The first experimental and commercial systems have demonstrated significant performance gains. But when performing floating-point arithmetic—calculations used extensively in scientific and technical applications—RISC machines made a lackluster showing. At least until now. Ridge Computers has dramatically improved floating-point performance in its second generation of RISC products, the 32/100 Series (Fig. 1)

TECHNOLOGY TO WATCH is a regular feature of *Electronics* aimed at providing readers with exclusive, in-depth reports from companies around the world on important technical innovations. It covers significant technology, processes, or developments incorporated in major new products. The reports also provide analyses of technical data, so that readers can assess the impact of new developments. John V. Sell, chief engineer of Ridge Computers, led the team that developed the RISC system described here. At VLSI Technology Inc., Andy Haines, Dan Yoder, and Ralph Naden worked on the Megacell and Megabus concept.

Versions of RISC developed in academic research projects are defined more rigidly in a number of papers than the two commercial RISC systems on the market. The earliest RISC was a research project at IBM Corp. in the early 1970s called the 801—a lean machine based on emitter-coupled logic with hardwired control and few single-cycle instructions. Then came two well-known and well-documented university projects—the RISC I and its follow-on RISC II processor chips at the University of California at Berkeley and the MIPS processor at Stanford University.

Besides having a much smaller number of simplified instructions compared with complex-instruction-set computers, RISC architectures also often include:

- A simplified and fixed instruction format, where the instructions are all the same size and have the same structure.
- Hard-wired control rather than microcode.
- Most, if not all, instructions operating in a single cycle.
- A design where only the load and store instructions access memory.

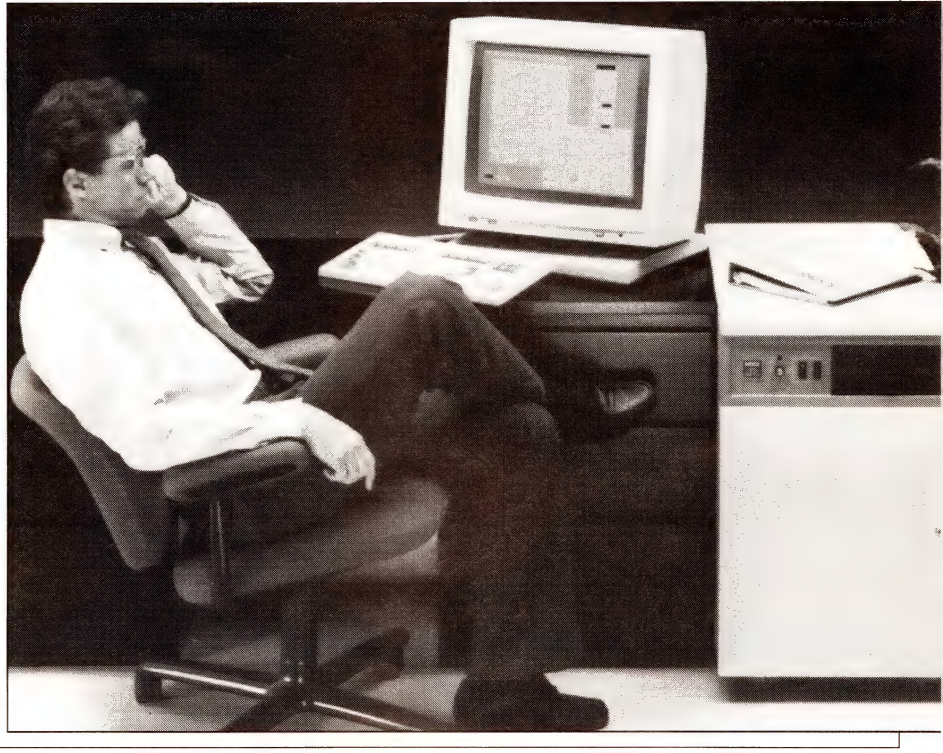
The RISC idea came about when research showed that on conventional machines, most complex instructions are executed infrequently. The results are close to the common 80-20 rule: 80% of the instructions are used only 20% of the time.

The early RISC researchers, such as John Cocke at IBM, who started the 801 project, and David Patterson at Berkeley, posited that a computer could probably operate faster if complex instructions were broken down to basic commands such as Load, Store, Branch, Compare, and Add—each of which could be executed in one clock cycle. With fewer instruction types to decode, RISC architectures require less hardware to implement. The result is better cost-performance ratios for RISC machines over conventional complex-instruction-set computers.

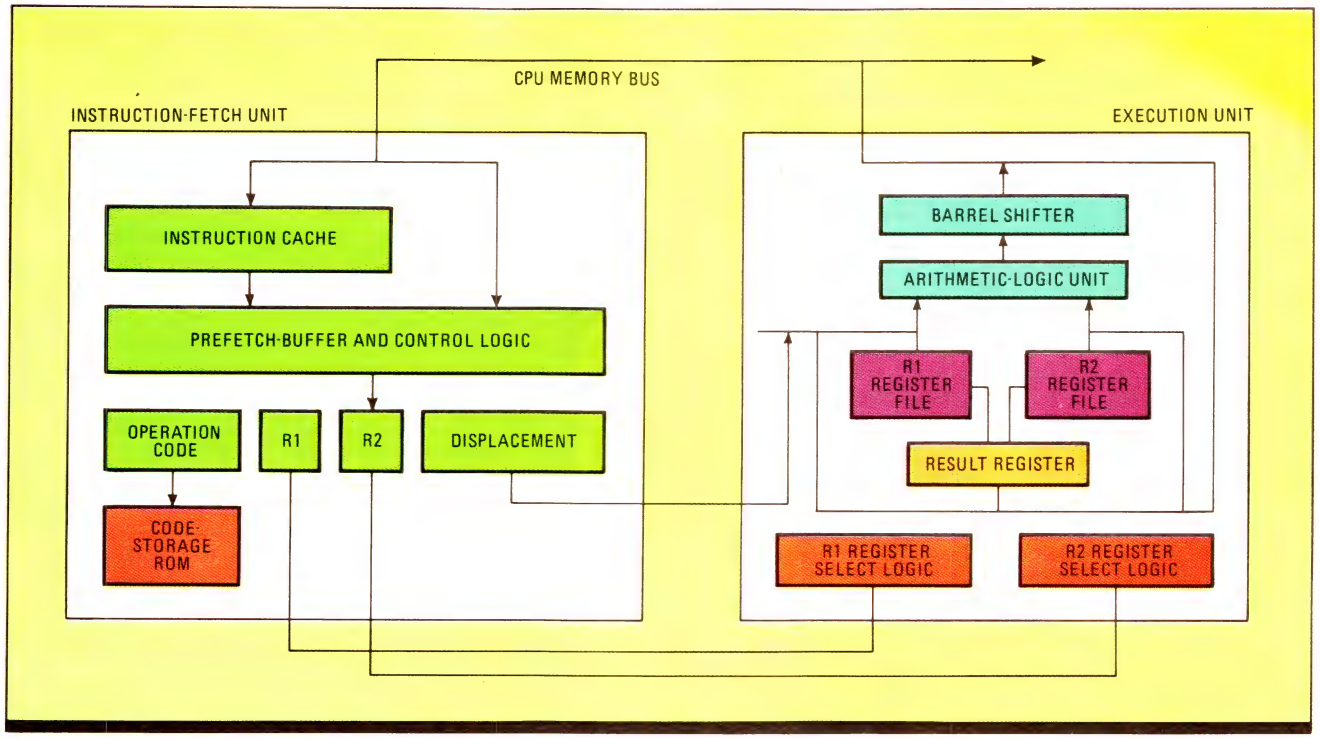
The complexity of floating-point instructions makes them unsuitable for efficient processing in a RISC architecture, so RISC machines typically offload these operations to separate special-purpose floating-point processors. The traditional RISC architecture takes too long to execute these instructions. "However, the floating-point bottleneck may have little to do with the architecture itself—only with its hardware implementation," says John V. Sell, chief engineer at Ridge.

The enhanced floating-point central processing unit developed for the 32-bit 32/100 series of superminicomputers recently introduced by the Santa Clara, Calif., firm performs all floating-point operations in its RISC CPU. Ridge has determined through running benchmark programs that the machine handles floating-point operations two to four times faster than its predecessor—performance good enough to beat a Digital Equipment Corp. VAX-11/780 on a finite-element-analysis test and to jump the Ridge up by 30 places in the Argonne National Laboratory's linear-equation sweepstakes.

Ridge has benchmarked its new machine against a VAX-



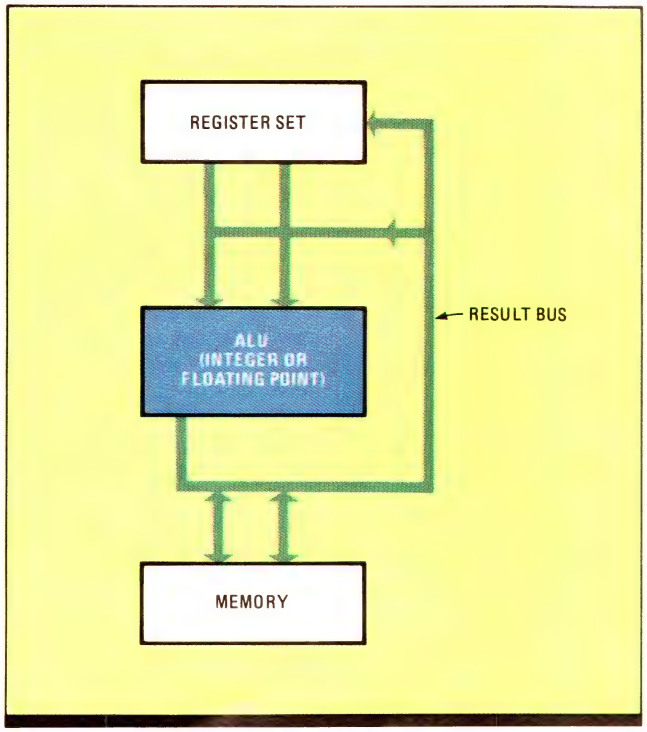
1. New RISC. The Ridge 32/100 reduced-instruction-set computers do computation-intensive jobs faster than previous models.



2. Simple structure. The internal structure of the Ridge 32-bit CPU consists of two simple parts, an instruction-fetch unit and an execution unit. Instruction formats are simple, consisting of an operation code and two register-file addresses either with or without displacement.

11/780 with a floating-point accelerator on the Ansys structure-analysis program. Offered by Swanson Analysis Systems Inc., Ansys is a large-scale general-purpose program that uses finite-element-anlysis techniques to solve several classes of engineering analysis problems. For a static analysis of 1,318 elements, 1,001 nodes, 3,001 degrees of freedom (the matrix size of the solution), and 284 wavefronts, Sell says the VAX took 6,994 CPU seconds versus 4,200 for the Ridge.

The Ridge processor also passed with flying colors when tested on the Linpak software, which has a high percentage of floating-point operations. The previous Ridge 32 computer took 10.0 s to compute a series of order 100, a rate of about 68,000 floating-point operations per second. The 32/330, using an optimizing compiler, took 4.58 s, or about 150,000 flops. A hand-coded version reduced that time to 3.26 s—about 210,000 flops.



3. Bypass. Because data may never need to be stored while calculating inside a loop, a results bus shunts it directly back to the arithmetic-logic unit. A single instruction can be repeated with no delays.

Argonne Laboratories developed Linpak as a standard Fortran benchmark for measuring performance in solving linear equations. The laboratory tested over 100 computers with Linpak. The fastest Ridge performance is approximately equal to that of a Denelcor Inc. Heterogeneous Element Processor and just under that of a hand-coded VAX-11/785 with a floating-point accelerator.

Ridge uses 91 instructions in its set, including a full set of floating-point instructions. It is theoretically possible, given enough hardware, to perform any of these instructions in one or two clock cycles (depending on the instruction length, which may be 16, 32, or 48 bits).

However, Ridge's floating-point-addition instruction takes five cycles, says Sell. Load and store operations, which require memory access, also take more than one cycle. Cutting the cycles per instruction to a minimum would add about 100 integrated circuits to the CPU—more hardware than Ridge could justify. The cost of adding hardware to increase the number of single-cycle instructions would outweigh the gain in performance.

Ridge's designers wanted to create a software environment in which the data space and the instruction set are what the compiler needs to turn a user program into efficient runnable code, Sell says. The Ridge system runs AT&T Bell Laboratories' Unix System V, with the Berkeley 4.2 enhancements. This operating system, however, is actually the user interface to Ridge's process-based message-passing system, in which each process "owns" the data it is working on. "This is a non-RISC approach in that

it is more complex in the physical implementation than when processes share memory," Sell says. "However, it allows greater modularity in system software, since each engineer can design his own piece of it and track where the data is modified."

The Ridge 32/100 uses general-purpose registers; two sets of registers carry out all data manipulation (Fig. 2). Where a memory-to-memory structure requires a sequence of instructions to fetch data, put it into the CPU, perform the operation, and return the results to memory, the Ridge computer performs only three instructions—a Load, a Do, and a Store.

Taking a shortcut

One criticism of the RISC approach is that the progams are longer and thus need more instructions per operation. But inside a loop, Sell points out, data may never need to be stored and a single instruction can be repeated with no delays. To accomplish this, Ridge has built a results bus into its CPU; the results bus returns data directly to the CPU without even passing through the register set (Fig. 3).

Conceptually, a Ridge floating-point-addition process looks the same as an integer addition. For example, the computer takes two values from two registers, R1 and R2, puts them through a black box called an adder, and stores the result in R1. The only difference between the two kinds of addition, Sell says, is that the floating-point adder and the integer adder are separate. Both, however, are implemented using small- and medium-scale ICs inside the CPU. In this way, the Ridge machine differs from typical RISC computers, which have been popularized by the very large-scale integration approach taken at Berkeley and Stanford.

Ridge gets its high performance by using high-speed Schottky TTL logic together with optimizing compilers. The VLSI chips designed at Berkeley and Stanford build RISC into silicon, which limits floating-point performance to what is feasible on a single chip.

Such structures need floating-point coprocessors, with their attendant offloading procedures, where Ridge can keep all operations in the same CPU. The Ridge processor consists of some 400 medium- and small-scale packages on two circuit boards, containing some 12,000 gates.

To make VLSI processors work requires that the arith metic-logic unit, the registers, and the memory controller be closely integrated, Sell says. The discrete approach allows more flexible timing. In addition, a separate floating-point processor loses the instruction overlap that is possible when all operations stay in the same CPU. The parallelism obtained with this approach makes it possible to reduce the floating-point-addition process from 32 clock cycles in the original Ridge machine to five in the 32/100. The first two cycles fetch 64-bit operands; the third adds them; the fourth and fifth normalize and adjust the result.

"We get higher performance by integrating everything into the same CPU than by trying to put it all on one chip," Sell says. However, he adds, the architecture can be adapted to high-performance VLSI processors; Ridge could opt for the next generation of 32-bit commercial microprocessors or even design its own chip. The present design could be implemented in currently available gate arrays, he notes.

Ridge markets its computers to technical organizations that need computationally intense equipment for three-dimensional modeling or for the inversion of arrays and matrices in simultaneous equations. □

MEGACELLS: A FASTER ROUTE TO SEMICUSTOM CHIP DESIGN

Very large-scale cells implement complex processor functions

The Megacell family of very large-scale CMOS microprocessor macrocells from VLSI Technology Inc., San Jose, Calif., is part of the continuing trend to lower system cost by placing as much capability as possible on the fewest chips. VTI's Andy Haines, strategic marketing manager of application-specific products, and Dan Yoder, manager of custom systems, say the Megacell approach provides a maximum level of integration while preserving the investment in software that many firms have made.

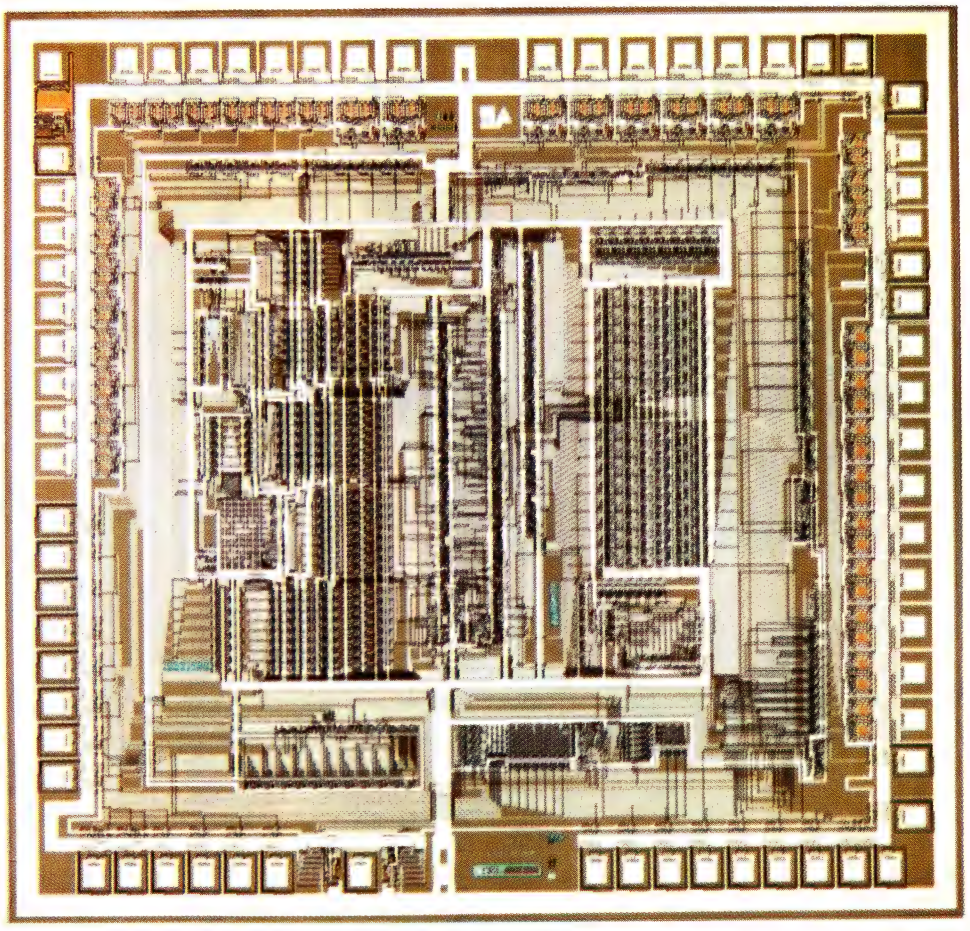
Megacells are a new type of technology for application-specific integrated circuits developed for the semicustom market. They are similar to standard cells in that they reside in a design system's data base and are called in as blocks to implement components identified within a schematic diagram. In addition, they function as standard cells in that the two types can be combined on a single chip to create more complex VLSI circuits that otherwise would take considerably more real estate. But Megacells, unlike smaller standard cells, represent thousands of logic gates that duplicate entire standard LSI microprocessor and peripheral functions, allowing rapid integration of systems and subsystems—such as disk controllers, counters, and microprocessors—within a single chip.

Thus the designer doesn't have to design the internal structure of the blocks, only interconnect them. Also, the designer is not constrained by the need to use off-chip components or tied up with a lengthy design process to obtain desired functions. This significantly reduces design times and makes possible cost-efficient, rapid development of complex VLSI devices, up to and including those that are complete single-chip systems. Although it is a faster process than full-custom design, it yields the same density.

Thanks to semiconductor-manufacturing techniques currently available and the increased level of integration

MEGACELLS DUPLICATE LARGE-SCALE FUNCTIONS

Identification	Description
6845	High-performance-MOS CRT controller
ROM	H-MOS 16-K, 32-K, 64-K, 128-K
82C54	CMOS counter/timer
82C84	CMOS clock generator
68C45	CMOS CRT controller
82C50	Universal asynchronous receiver/transmitter
82C59	Interrupt controller
82C55	CMOS parallel I/O port
82C88	CMOS bus controller
82C37A	CMOS direct-memory-access controller
16C450	Advanced UART
65C02	CMOS microprocessor



1. Megacontroller. Designers can combine Megacells with additional logic to yield custom chips. A CRT controller for a computer was thus designed with VTI's 6845 Megacell and user-specific logic.

possible, many popular large-scale peripheral chips that were originally implemented in 3- or 4-μm high-performance MOS can be replaced by 2-μm CMOS VLSI chips to produce smaller, faster, and more economical systems. But the large software base that has been developed for the existing microprocessor systems represents a major investment that can be retained only through preserving software compatibility. With this in mind, VTI designed Megacells to integrate complete functions while preserving compatibility with existing products. By turning functions contained on boards into single chips with Megacells, VTI designers ensured that both the hardware and software remain compatible with the previous design.

Multiple Megacells can be incorporated onto a single IC to provide the standard-cell-level functions with which the designer is familiar. The procedure is similar to using standard cells, and is therefore easy for microprocessor designers to use. This system-level integration offers VLSI benefits such as reduced engineering and design time, smaller dice, lower production costs, and faster turnaround time, besides protecting the software investment.

For example, VTI recently completed development of the VGC6845 cathode-ray-tube controller, based on a Megacell that fully implements the widely used 6845 device, to be used in a computer (Fig. 1). This chip is the equivalent of a complete CRT controller board containing 64 ICs and allows use of all the extensive software in existence for the first-generation system, in addition to offering the VLSI advantages of size and speed.

Megacell design tools

To improve design productivity and ensure first-time silicon success, VTI has developed Megacell-specific tools that complement the existing schematic entry, net-list extraction, test-pattern generation, and other end-to-end design capabilities of the firm's silicon compilers and chip-design tools.

Megacells are not currently available for all possible applications, but a designer can add standard cells to implement custom functions. For example, an 82C54 timer-counter and a 82C55 parallel input/output port can be combined with a standard-cell implementation of a direct-memory-access controller in designing an application-specific peripheral.

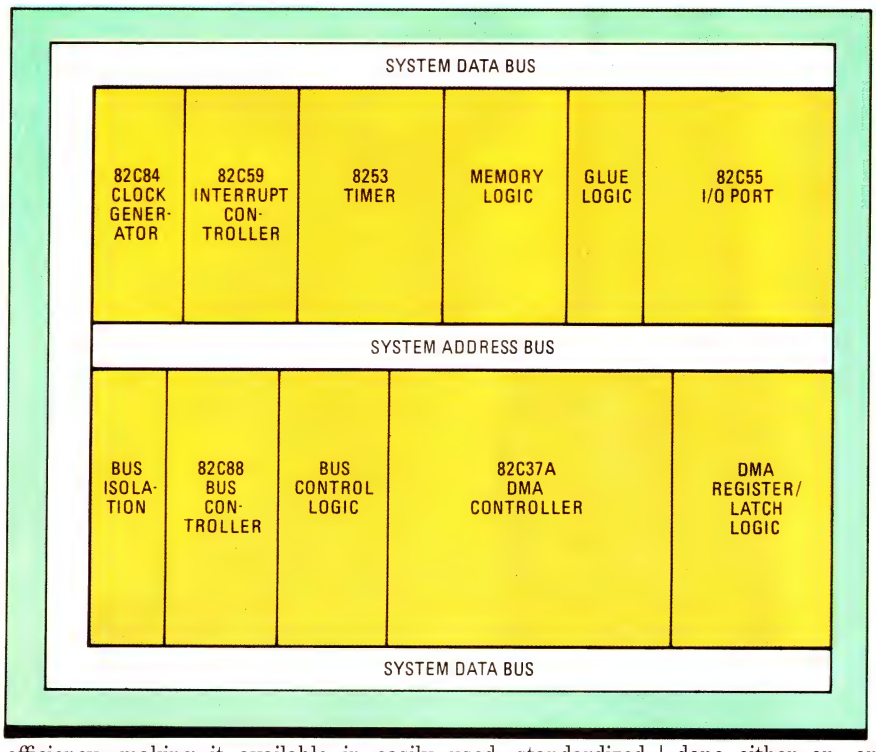
A common method of implementing a semicustom chip design is to simply remove the bonding pads from standard LSI devices and enter the result into a cell library. This creates VLSI cells that have physical structures similar to the different-size standard chips from which they are developed, with the rectangular die shape intended for bonding into a dual in-line package generally retained. Such an arrangement may seem advantageous from the vendor's point of view. But a structure that is optimized for bonding into a DIP is not optimized for integration with other circuitry on a VLSI chip. The problem is the irregular structures of the cells. Several such structures combined on a chip could lead to megaholes.

Megaholes are areas of wasted silicon real estate that result from trying to create a regular structure with irregularly shaped functional blocks. Wiring constraints, for example, may preclude certain configurations, or there may not be a block of the proper size for an available space. This can be a particular problem when combining different cell types with multiple random-size geometries.

Alternatively, a designer can develop a Megacell-like structure from net lists using a standard-cell library; when the designer runs a net list on a work station or host computer, a predetermined function is compiled from the specified cells. This effectively creates a Megacell, in that the designer produces a complete function with a single call. But it actually results in a standard-cell configuration. And because the routing channels associated with standard cells are large, such an approach exacts a penalty in silicon area. It also makes the efficient use of multiple Megacells more difficult and unnecessarily increases the product cost because fewer functions can be incorporated into the chip.

Megacell developers have taken the approach of completely redesigning LSI functions to conform to a standard bus structure and with standard dimensions rather than attempting to modify existing designs through an intermediate technology, such as standard cells. The cells in the firm's Megacell library vary only in width; therefore, a designer can organize them in an orderly manner that conserves real estate and simplifies chip layout. Megaholes and wasted space in large routing channels thus cease to be a concern, because the cells fit neatly together.

In creating Megacells in this way, VTI has done the full-custom design necessary for optimum performance and silicon



2. Playing with blocks. The regular structure and straightforward nature of VTI's Megacells and Megabus allow integration of complete board-level functions into a single-chip VLSI motherboard for a personal computer.

efficiency, making it available in easily used, standardized functional blocks, says Ralph Naden, director of software operations. He believes the approach offers the benefits of both full-custom and standard-cell technologies without the schedule and development cost penalties of the full-custom route or the silicon-efficiency penalties of standard cells.

Other ways to implement Megacell-type structures raise problems. A difficulty with standard-cell implementations, especially those that use net lists, is that they must be rerouted every time they are used. This also means that the "Megacells" must be recharacterized each time, which in turn makes standardization difficult, if not impossible, and may require modification of test programs.

Because their structure is set, Megacells need not be rerouted for inclusion on a chip. And like the standard functional blocks they implement, all Megacells are fully characterized in that all parameters are known for each function and remain constant for any application. For instance, the 6845 Megacell has the same performance data as that provided by the manufacturer of a standard 6845 device and ensures the user that the data is valid regardless of the configuration in which it is used. As further assurance that Megacell operation is what the user requires, a physical evaluation chip is pinned out in exactly the same way as the standard product. Rather than simply permitting simulation of its cells, VTI provides the evaluation chip for running on a tester, so the user can run actual application code.

Functional testing

Because of the consistency of structure and performance of each functional Megacell, VTI developed a test language as part of the company's tool package. The user can put each cell into a test mode that allows testing from the pad ring, employing customer-provided logic. Each function can be tested as though it were a stand-alone chip, ensuring performance at each step in the design process. For example, functional simulation models are available that enable circuit simulation of chips containing multiple Megacells and compiled cells. With performance of the peripherals verified, the designer needs only to do further tests on the associated on-chip logic (in a typical application, from 500 to 1,000 gates are adjacent to the Megacell for logic and other functions). This reduces overall test time and also encourages the designer to break the logic into functional, testable blocks.

For greater testability and ensurance of first-time design success, VTI has functional models of Megacell products available for simulation at the functional level, rather than on the gate or transistor level. These models will run on engineering work stations, reducing the computer power—and related expenses—required for the design process.

To further optimize chip area and design time, designers can interconnect Megacells with other Megacells and on-chip standard cells by means of a novel address and data bus structure called Megabus. Megabus is conceptually very straightforward: it is a high-speed synchronous bus that has predefined signals, timing, and physical locations for the address and data lines. Addressing can be done either on- or off-chip; on-chip address decoding eliminates the need for external decoder chips.

In creating Megacells, VTI defined standardized physical locations for signals that place I/O channels on the top and bottom to facilitate connection to the buses. Where it is considered most effective, however, signals can enter and leave the sides of the cells. Connections from the cells to the chip's pad ring are routed under the Megabus structures. Glue logic, residing in the design system's data base, can be built into the pad ring to provide translation for memory read/write operations and to interface with external buses. All the lines drive standard loads so that as many as nine Megacells can be put on a single chip, depending upon such considerations as the bus-transfer rate.

Fast and flexible

Megabus speed is optimized by its synchronous nature, which makes it inherently faster than an asynchronous bus. Bus transfers of up to 3 MHz are now supported, which is comparable to a system clock frequency of 10 MHz for an 8086 microprocessor. This allows the Megabus to cover the widest range of microprocessors, from such older products as the 6502, Z80, and 8085 to such newer processors as the 8086, 8088, and 68000. It also ensures that the user of the Megacell peripherals will not be tied to any one processor.

It is extremely easy for system-level designers to use Megacells because Megabus timing waveforms for the various functions have the same shapes and sequences as the corresponding standard products. But they are faster. General performance improvements of 50% to 75% have been realized as a result of implementation in VTI's advanced 2-μm double-metal CMOS process.

The layout of a single-chip version of a personal computer motherboard (Fig. 2) shows how Megacells can implement complete board-level functions in one VLSI circuit. With the exception of the microprocessor and mass memory, all the basic computer peripheral functions are present in this version. Because the individual functional blocks can be called by icon from the data base, design time is significantly less than would be necessary if they were developed individually, and silicon efficiency is greater than would be possible with standard-cell implementations. □

ADA ENTERS THE WORLD OF PARALLEL MULTICOMPUTING

Flex/32 puts supermini muscle behind the Defense Department's language

Ada, the high-level language used by the Defense Department to provide a uniform programming environment, is marching into parallel multicomputing. At this week's National Computer Conference, Flexible Computer Corp. is unveiling what it calls the first commercial use of Ada in a multicomputer system, called the Flex/32.

Flexible Computer believes parallel multicomputing based on Ada will help propel the emerging programming language to projected annual sales of more than $1 billion in three years. Market researcher International Resources Development, Norwalk, Conn., projects that Ada software sales will reach $360 million this year compared with only $250 million last year.

The Flex/32 Ada concurrent-processing development system is based on a programming language compiler licensed from Verdix Corp., McLean, Va. With Flexible Computer's Ada system, software developers can create and debug parallel-processing programs on a single computer, which simulates the multicomputing environment. The Flex/32 hardware is based on the 32032 microprocessor family from National Semiconductor Corp. and has been designed to exploit concurrent operation on multiple, independent computers with parallel data buses [*ElectronicsWeek*, May 13, 1985, p. 49].

Once the Ada programs have been debugged, they can be gradually transferred to a real-time environment using the Flex/32 multiple processor and bus architecture, says Ray Naeini, vice president of software development. In creating the Ada package, Flexible Computer used the same program development philosophy as in its existing software environments—Concurrent C and Concurrent Fortran.

Unix execution. As with Flexible Computer's other concurrent languages, the system executes Ada program development under Unix System V. A concurrency simulator package then debugs and corrects programs while programs are running on a single 32-bit computer.

During program development, Ada programs can be executed under Unix, the concurrency simulator, or in real-time under Flexible Computer's own MMOS—for multicomputing, multitasking operating system. "This all goes along with the same approach we are providing with our other environments. Using our tools, users can select the appropriate environment," says Naeini. "If a program has no bugs, all that has to be done to define a new environment is change a single command." For example, by changing the command it can automatically map programs into the Flex/32 multicomputer local memory.

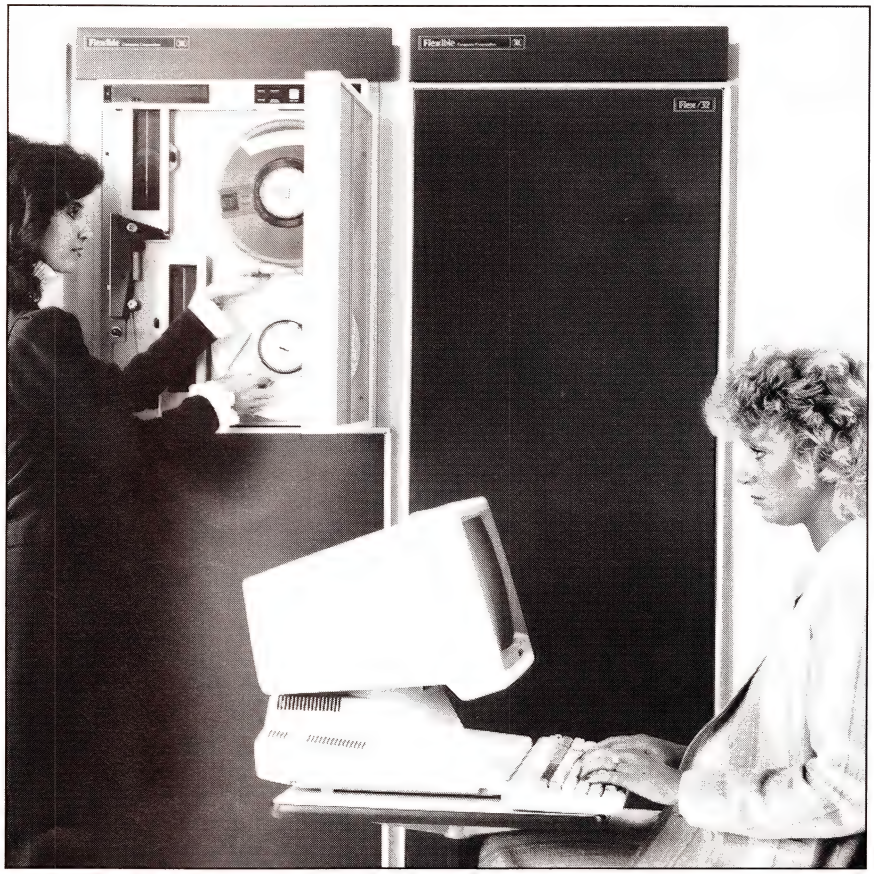
NCC PRODUCT ROUNDUP

Far fewer products will bow at this year's National Computer Conference than in recent years. Market conditions have even prompted some companies to skip the show, in Chicago this week [*Electronics*, July 8, 1985, p. 17]. Nonetheless, these four-plus pages present nine of the most significant offerings.

The Flex/32 Ada system uses the language's embedded parallel-processing support, known as rendezvous signaling, to perform messaging between computers. Both the Flex/32 hardware and MMOS operating system support this synchronization with system calls and concurrency syntax. From 2 to 20 directly programmable 32-bit minicomputers with shared and local memory can be loaded into each Flex/32 cabinet. More than 1,000 cabinets can be configured into one massively parallel system.

Flexible Computer chose an Ada compiler package from Verdix because it has DOD validation. Also, it contained a modular structure, so it was easily adapted to the multicomputer architecture. The Verdix Ada Development System (VADS) contains a high-speed Ada compiler, an interactive screen-oriented debugger, library-management tools, and run-time system.

In modifying VADS, Flexible Computer expanded the compiler so that users could program each computer. "In an Ada program, you can allocate tasks to



Parallel. Flexible Computer has modified Ada to run on its multicomputer system.

the actual computer you have available in the configuration. This is an option, otherwise the system can select it automatically with a load-balancing environment," explains Naeini.

The second and most important task in readying the Flex/32 Ada package was making the language executable under MMOS, which supports real-time execution plus concurrent processes on multiple computers.

Deliveries of the Flex/32 Ada package will begin in September. A typical two-computer Flex/32 system with peripherals and Ada development tools sells for $175,000. *–J. Robert Lineback*

Flexible Computer Corp., 1801 Royal Lane, Suite 810, Dallas, Texas 75229. Phone (214) 869-1234 [Circle reader service number 400]

GAS-PLASMA PANELS BUILD LARGE DISPLAYS

Combining modular construction and a thick-film ink composition that can handle high-current densities, Quantum dc gas-plasma displays feature 2-in. characters for large information panels of up to 7 by 11 ft. The neon-orange-colored flat-panel displays are for use where information must be displayed to large audiences, such as in space and military command centers, data-processing operations, lobbies, airports, and stock exchanges.

Quantum displays are made up of individual panels that the user can stack and arrange end-to-end. Each dot-matrix plasma module has its own drive electronics mounted on a pc-board attached to its back. The driver boards are based on Zilog Z80 8-bit microprocessors, supported by serial and parallel I/O components as well as by CMOS high-voltage circuits from Sprague Electric.

Each panel module fits into a metal holder that aligns the display building-block onto a backplane. The 2-in.-character display consists of up to one row of 8-character blocks. The largest standard configuration offered is 24 lines by 80 columns, or 1,920 characters.

"When people look at these finished displays, they think they are looking at a single display panel. That's because the matrix-format design provides proportionate spacing between alphanumeric characters on each side of the abutted panels," says Charles Odom, president of Applied Micros. The abutted plasma panels are covered with an acrylic wall that acts as an amber filter, giving the appearance of a single flat-wall display.

"It is not possible to build a monolithic gas-plasma panel the size of these displays because the production equipment is not available," explains Odom. And conventional computer displays, such as CRTs, are not effective 100 feet away, he adds.

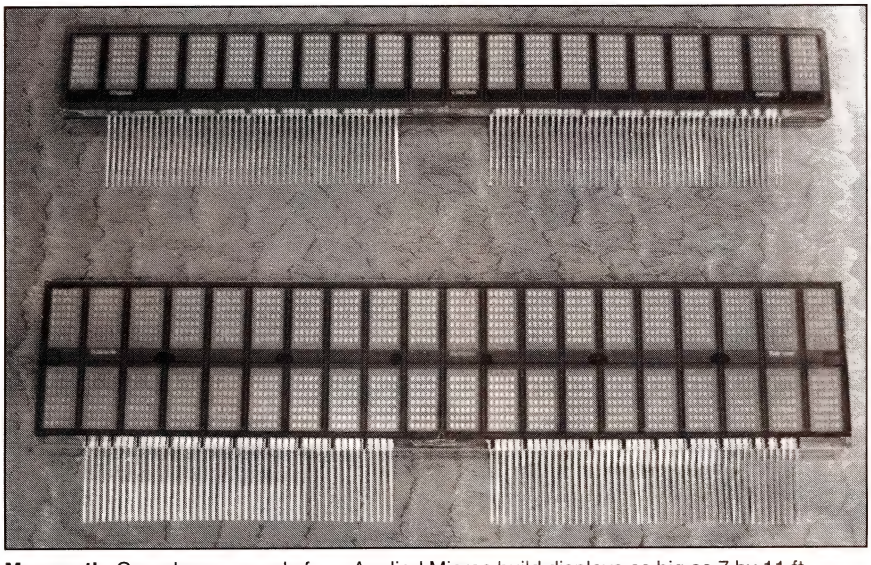
Including power supply and casing, a complete 7-by-11-ft plasma display (1,920 characters 2 in. high) costs $105,000 with deliveries slated 90 days after order. But, because of the modular construction, customers can order smaller 2-in. displays for much less money, says Odom. A two-line 40-character configuration sells for $4,500; a one-line 8-column panel is $1,300.

The modular panel-assembly technique—licensed from developer Quantum Electronics Inc.—is also being used to make 1-in.-character plasma displays for similar market needs. These displays are constructed from two-line 20-character and one-line 20-character sections. Standard 1-in.-character displays can be assembled into panels as large as 4 by 6 ft, providing 24 lines by 80 columns.

Custom plasma displays can be made by combining the new 2-in.-character panels and the year-old 1-in.-character panels, says Kit Kennedy, president of Quantum Electronics. "We manufacture our own thick-film inks, which are durable with a large current density," says Kennedy. The ink will not sputter with the high currents needed to illuminate the large characters.

A 24-line 80-column panel of 2-in. characters will require 110 V and 60 A. The 1-in. displays run from a 110-V supply rated at 20 A. *–J. R. L.*

Applied Micros Inc., 550 Julie Rivers Dr., Suite 100, Sugar Land, Texas 77478. Phone (713) 240-5555 [Circle 402]



Mammoth. Gas-plasma panels from Applied Micros build displays as big as 7 by 11 ft.

GRAPHICS CARD BOWS FOR CAD/CAM

A graphics display controller with a 1,024-by-1,024-pixel memory for high-resolution color graphics occupies a pivotal position in Motorola Inc.'s VME-system microcomputer family. A two-board set, the MVME390 may be used for red-green-blue or monochrome monitors with analog video input.

"This controller is important in expanding the VMEsystem products into applications requiring high- to medium-resolution displays," says Bruce Crozier, the line's product planner at Microsystems Operation, Tempe, Ariz. Principal uses are expected to be industrial process control and computer-aided design and manufacturing. Motorola offers more than 40 of the 68000-based VME-bus-system modules to manufacturers, and is adding more.

The new module's display format is configurable for most standard monitors, from the board's full resolution of 1,024 by 1,024 pixels down to 512 by 380, in square or rectangular format. The memory consists of 384-K bytes of video RAM, which is dual-ported to the VME-bus and to the display refresh logic.

Memory is organized as three planes of 1,024 by 1,024 pixels, which permits it to simultaneously produce eight colors from a palette of 4,096 or eight gray-scale levels from a range of 16 for monochrome displays. Thanks to flexible addressing, the memory can be accessed from the VMEbus on either a bit-plane or pixel-by-pixel basis.

For flicker-free display in high-performance operation, a noninterlaced 60-Hz refresh rate permits use of monitors with standard persistence phosphors,

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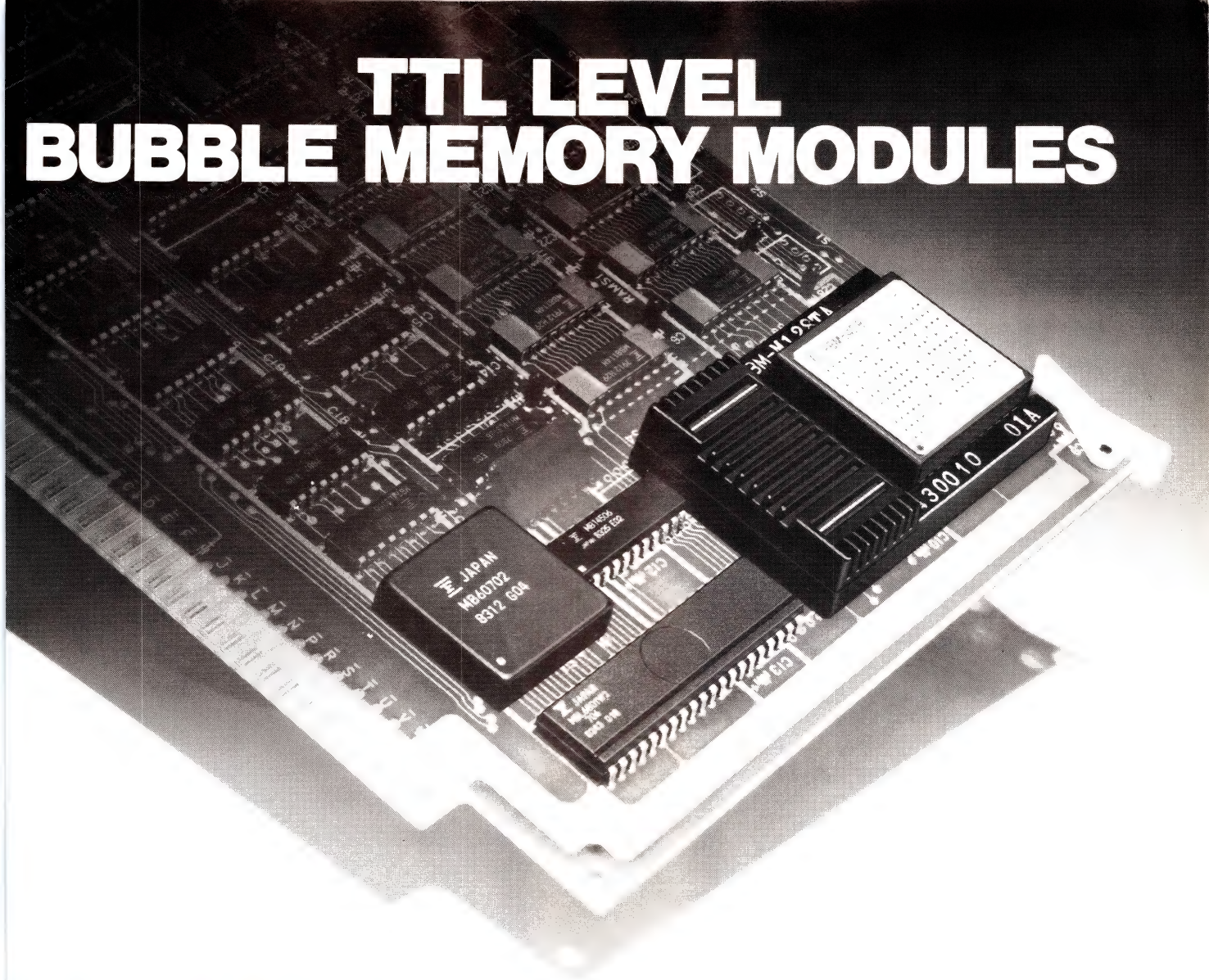

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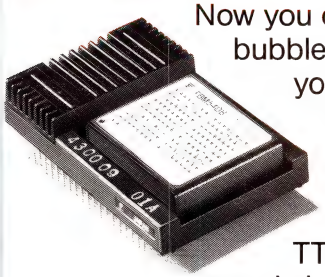

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Weight	75g	
Dimensions	43.5 x 65.5 x 13.7mm	

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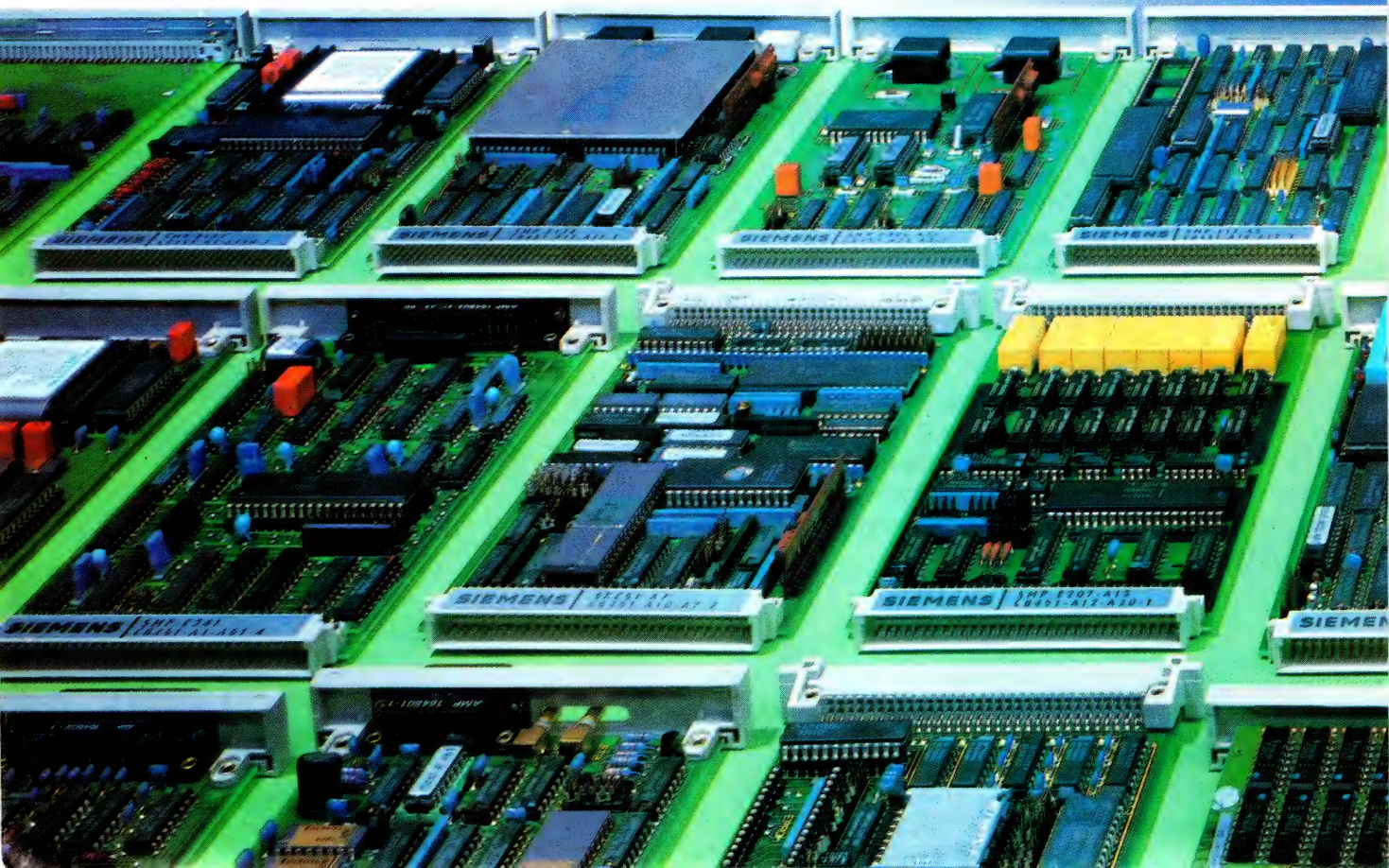

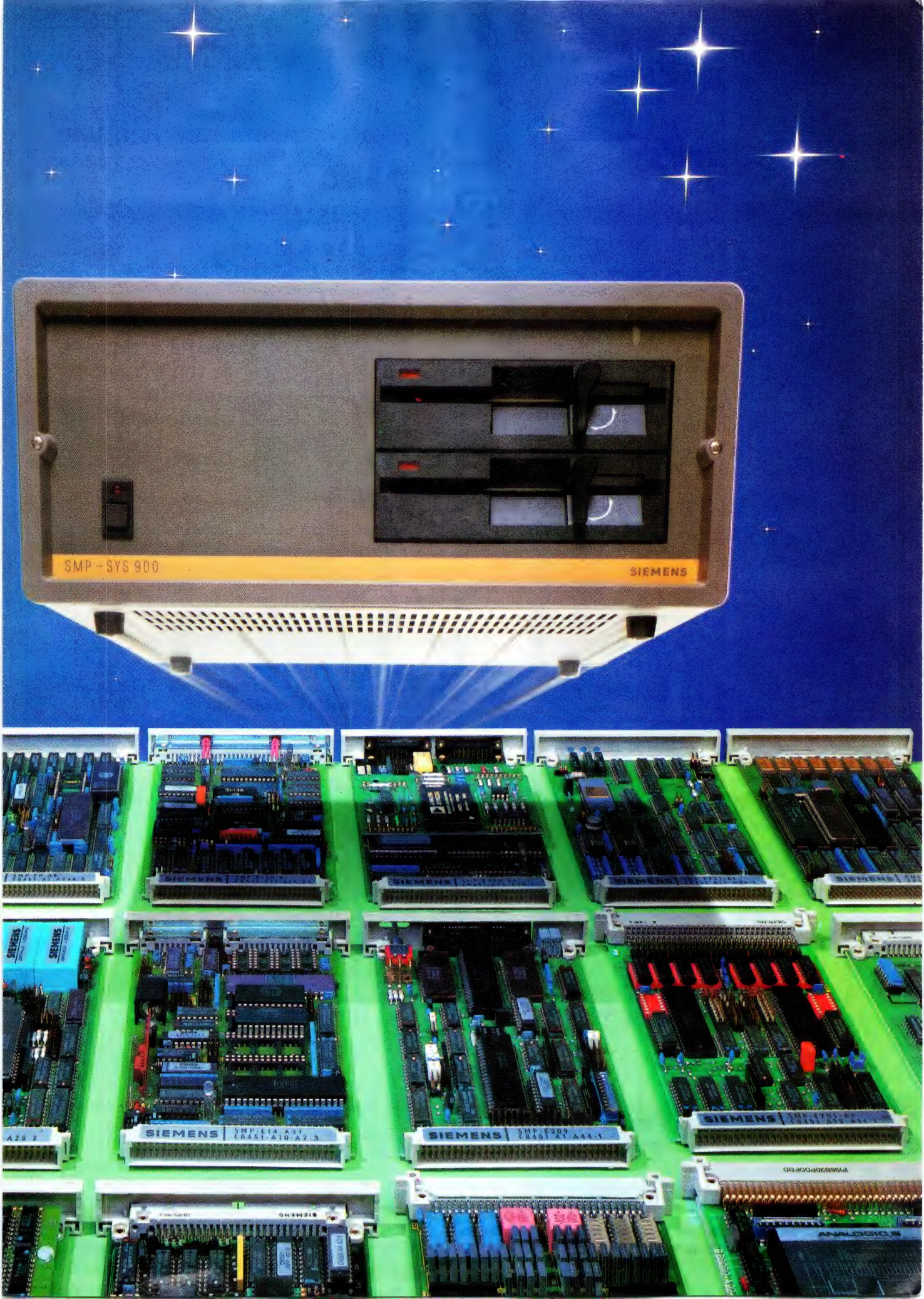
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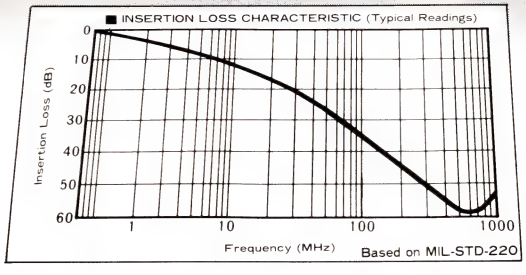

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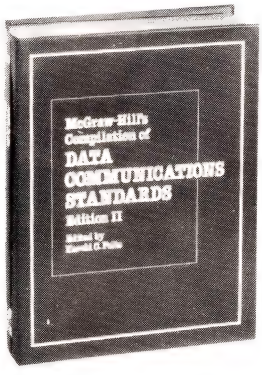

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which allows changing data quickly without smearing. This feature also improves display definition, according to the company.

Video RAM is available to the VMEbus 95% of the time, even when display-refresh logic operates at maximum speed and resolution or rewrites all pixels 60 times/s, putting one pixel in every 16 ns. The board needs to make a memory read cycle only once every 16 μs. The memory is designed so that the refresh logic can read a complete line in one read cycle, into an internal high-speed shift register. The video RAM is then available for VMEbus accesses while the current line is being sent to the display, according to the controller specifications.

This feature confers several advantages, chiefly that image updates can be written into the display memory more quickly. Further, the display does not break up when a new image is being written, and it is not necessary to restrict access to the memory during short horizontal/vertical-retrace/blanking intervals.

For different monitors, users may reconfigure the MVME390 by installing the appropriate dot-clock crystal and setting the desired display parameters in software. Practically any combination of the three parameters that specifiy resolution may be selected: resolution, refresh frequency, and interlace mode.

Pricing of the two-board set is $4,500; each sells separately for $2,300 because the MVME390-1 baseboard can be used alone for binary TTL monochrome monitors and the -2 board adds two more bit planes. The VME graphics display controller goes into beta-site testing during August and is scheduled for production in October. *–Larry Waller*

Motorola Microsystems Operation, 2900 South Diablo Way, Tempe, Ariz. 85282. Phone (602) 438-3516 [Circle 401]

SHUTTER BRIGHTENS PC AT DISPLAY

The Liquid Crystal Shutter Group of Tektronix Inc., applying technology announced in February, is introducing its first product at the NCC—the LCS Professional Color Graphics System for the IBM Corp. Personal Computer AT.

The system consists of the LCS 1220 color graphics display, the LCS C480 color graphics controller card, and the LCS E480 emulator card. Though the Tektronix 5116 oscilloscope and work stations made by its CAE Systems subsidiary use the shutter technology, this system adapts the technology for a product outside the company's line.

The display uses a 12-in. diagonal monochrome CRT monitor with 13-mil spot size. The shutter, made of a fast liquid-crystal optical switch sandwiched between two color polarizers and a neutral polarizer, gives the display a high contrast—15 : 1 (lightest to darkest). Based on the small monochrome spot size, it also has high resolution of 640 by 480 pixels. Because a single electron beam does the screen writing, the display lacks the fuzziness of typical shadow-mask color displays. Of the palette's 65,000 colors, the user can select 16.

The LCS C480 color graphics controller card fits the standard PC AT card form factor. It has a drawing speed (at 4 bits/pixel) of about 6,000 to 8,000 vectors/s. Alternatively, it can perform at 8 bits/pixel and has enough memory to store either 512,000 or 2 million pixels.

With the LCS E480 emulator card, the display can support the existing software for the PC AT and convert 200-line software—such as Lotus's 1-2-3, VisiCalc, and Multimate—into a 480-line display. Ordered in single units, the system sells for $3,900; it will be available in October. *–Eve Bennett*

Tektronix Inc., P.O. Box 500, MS 46-556, Beaverton, Ore. 97077.
Phone (503) 627-5000 [Circle 404]

LAPTOP COMPUTERS GET TINY PERIPHERALS

A microfloppy-disk drive and inkjet printer are compact, lightweight peripherals for Epson America's portable computers. The OEM Products Division has a 3½-in. SMD-280 disk drive that provides up to 1 megabyte of unformatted storage, measures 1.1 in. high, 5.8 in. deep, and 4 in. wide. It weighs under 1 lb. The HS-80 on-demand printer, weighing 3.6 lb, is 13.7 in. wide by 4.5 in. deep by 3.2 in. high.

Both peripherals are key additions to Epson's line for original-equipment manufacturers, to serve the growing number of small computers, says Jack Confrey, director of marketing for the division. "The SMD-280 has the capacity and performance of a much larger drive, but its size and power specifications open up a new range of applications." The HS-80 printer "fills out our portable product line in a significant way."

The drive consumes just 0.05 W in standby mode and uses 1.6 W during read and write operations. The microfloppy-disk drive has a track-to-track access time of 3 μs.

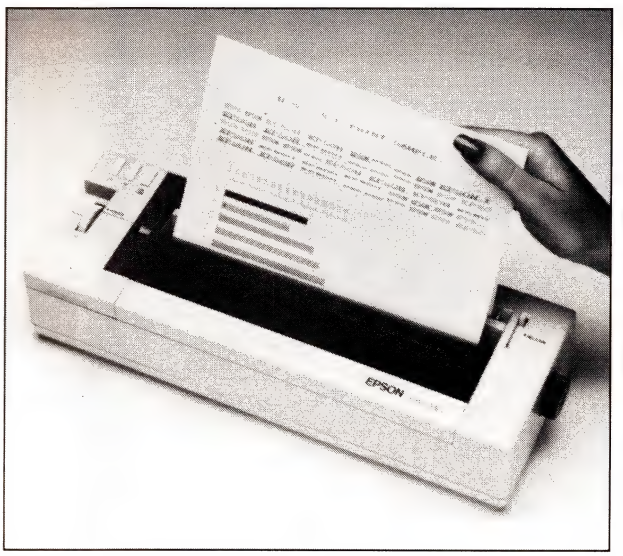
The unit's direct-drive motor operates from a 5-V power supply. Confrey says the credit goes to Epson's materials-research department for the low power requirements. The department developed special rare-earth magnets of high inherent force that require little power to drive the motor.

The drive accepts standard 3½-in. microfloppy disks of 80 tracks/s. Recording is performed at a density of 8,720 bits/in. and data is transferred at 250 kb/s. Automatic loading and unloading of disks is an option. "This means systems makers can pack a megabyte of storage into a battery-operated portable," Confrey adds.

The HS-80 printer uses a nine-nozzle print head and prints at speeds of 192 characters/s of Elite type, 160 c/s Pica, and 30 c/s letter-quality Pica. Needing no special paper, it prints sharply on most plain stock.

The Epson printer has a bit-image graphics-printing mode of 480 dots per line (normal density) with dots measuring 1/60 in. high by 1/72 in. across. At 960 dots per line (double density), the dots are 1/120 in. high and 1/72 in. across. Line spacing, which is programmable, is 1/6 or 1/8 in. An input data buffer of 256 bytes comes with the printer, which uses a parallel Centronics pin-compatible interface.

The printer has a refillable ink cartridge that prints about 200,000 charac-



Handy. Epson's small inkjet printer cranks out 192 characters/s.

ters. The user can refill the cartridge with a syringe.

The SMD-280 drive sells for $75 apiece in quantities of 10,000. The HS-80 printer, which sells for $449, is aimed at systems integrators. Both are available now. *–Larry Waller*

Epson America Inc., OEM Products Division, 23600 Telo Ave., Torrance, Calif. 90505. Phone (213) 534-4500 [Circle 405]

15-IN. VDT MEETS CAD NEEDS

The 19-in. work-station monitor may have competition in the market for computer-aided-design products. Nissei Sangyo America has just introduced a new 15-in. high-resolution color monitor—with pixels measuring 0.28 by 0.28 mm—that is small enough for desktop use and costs less than conventional 19-in. models.

"With this monitor, it is more feasible for each engineer to have his own system," says Dominic Cucé, Nissei's eastern region sales manager. The CM1588A monitor uses a standard 15-in. picture tube from Hitachi Ltd. and measures 14.4 in. wide by 12.8 in. high by 16 in. deep. The display screen measures 10.6 in. horizontally by 8 in. vertically. The video bandwidth is set at 80 MHz.

Although Cucé concedes that the monitor's resolution of 1,024 by 800 pixels falls short of its 19-in. counterparts', it far surpasses that of the 13-in. desktop monitors now available. The scan frequency responsible for the display is 50 kHz. The work-station monitors are available with a four-month lead time. The price per unit is approximately $2,100, including air shipping from Japan. In lots of 1,000 pieces, the monitors sell for $1,300 each. *–Debra Michals*

Nissei Sangyo America Ltd., 40 Washington St., Wellesley Hills, Mass. 02181. Phone (617) 237-9643 [Circle 407]

LOW-COST MICRO HITS OEM MARKET

The biggest bang for the buck. That's what original-equipment manufacturers and value-added resellers look for in a microcomputer system, and that's what Sord Computer of America Inc. claims to offer in its M68MX 68000-based personal computer.

Sord, a $100 million company, wants to expand its OEM and value-added reseller sales base in the U.S. by broadening its product line. The M68MX joins the dual-processor M68, introduced a year ago, and other higher-end products to give the company the breadth it thinks it needs to compete in the cut-throat OEM marketplace.

The M68MX comes with 512-K bytes of RAM and a high-speed 10-MHz 68000 microprocessor. It also sells for under $2,000, and that may be its best feature of all. Built in Japan and running under Digital Research's CP/M-68K operating system, the Sord computer supports a range of high-level languages such as C, R/M Cobol, Fortran 77, APL, Pascal, Lisp, Assembly, and others. Application programs, including word processors and spreadsheets, are also available. Regulos, an AT&T-licensed Unix-compatible operating system, will also be available, but the company will not say when.

A pair of 1.2-megabyte, 5¼-in. floppy-disk drives is standard. Available options with the M68MX include up to 4 megabytes of dynamic RAM, 640-by-500-pixel graphics in 16 colors, and a choice of either a high-density, 1.2-megabyte, 5¼-in. floppy-disk drive or a hard-disk drive with 10-, 20-, or 40-megabyte capacity. *–Tobias S. Naegele*

Sord Computer of America Inc., 645 Fifth Ave., New York, N.Y. 10022. Phone (212) 759-0140 [Circle 406]

SMALL WINCHESTER ACCESSES IN 40 MS

For its initial venture into half-height 5¼-in. Winchester disk drives, Computer Memories is unveiling two 20-megabyte (formatted) models. Their primary difference is speed: the CM3426, which is priced at just $400 each in original-equipment-manufacturer quantities, boasts an 85-ms access time; the faster CM4426, which carries a $650 price tag, accesses memory in 40 ms.

"The CM3000 and CM4000 series drives are targeted for the personal computer market, where size and price are critical," says Joseph Lloyd, the firm's manager of product marketing.

According to Computer Memories, the CM4426 is designed for applications that require 20 megabytes of formatted storage yet demand the high-performance, under-40-ms average access time. The company points to the target market of the most sophisticated of the new generation of desktop compact systems.

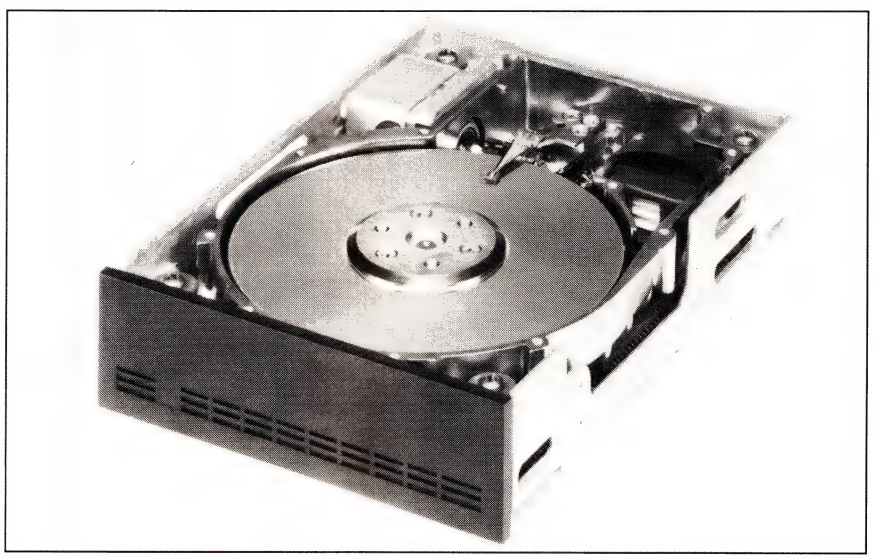
System integration is simplified by its industry-standard ST506/412 interface, half-height mounting, and low power consumption. The CM4426's performance and reliability come from such features as its isolated shock-mounted head-and-disk assembly, dynamic spindle brake, and dedicated shipping zone to park heads.

Both the CM4000 and CM3000 series drives feature a linear head-positioning mechanism with a stainless-steel band. Both also have high-output Winchester-type read/write heads. The heads are attached to a precision ball-bearing, three-point, self-aligning carriage.

The CM3426 offers high performance through a combination of a high-torque precision stepper motor, an on-board microprocessor, a crystal-controlled spindle drive, and high-output heads. It uses a stepper-motor linear band actuator and associated electronics to attain a track density of 606 tracks/in.

A delayed motor-start option is available. A read preamplifier within the head-disk assembly reduces susceptibility to electromagnetic and radio-frequency interference. Shock and vibration specifications exceed industry standards, says the company.

The drive is interchangeable with industry-standard, 5¼-in. floppy-disk drives having the same dimensions and



Thin. Computer Memories' drive combines small size with high capacity.

power requirements. What's more, the drive has been designed so that it can be mounted in any orientation.

The 3.35-lb CM3426 and CM4426 half-height drives measure 1.6 in. high by 5.7 in. wide by 8.0 in. deep. The CM3000 is available in original-equipment-manufacturer quantities now, and the CM4000 will go into volume production next month. *–Larry Waller*

Computer Memories Inc. 9216 Eton Ave., Chatsworth, Calif. 91311.
Phone (818) 709-6445 [Circle 403]

PC KEYBOARD HAS LED INDICATORS

The PC-122, a low-profile encoded keyboard from Hi-Tek Corp., has more timesaving function keys than IBM Corp. Personal Computer and PC AT keyboards. The PC-122 also has LED indicators in the number lock, scroll lock, and caps lock keys, so a user can see instantly if the keys are in their locked position.

The PC-122 was designed to easily accommodate an extra four keys around the cursor pad. The extra keys offer more freedom and flexibility, the company says.

"The PC-122 is an IBM 3270 look-alike, introduced because of growing interest from prospects and our current customer base over the last 12 months," says Kent Kimball, sales and marketing manager. "It will be used not only on units emulating 3270 systems but also for many non-3270 applications."

The PC-122 uses the Hi-Tek 725 series key-switch technology, which has a passive-contact system that isolates the contact force from the actuation force. The 725 series mechanical key-switch design has undergone over 100 million test cycles, the company claims.

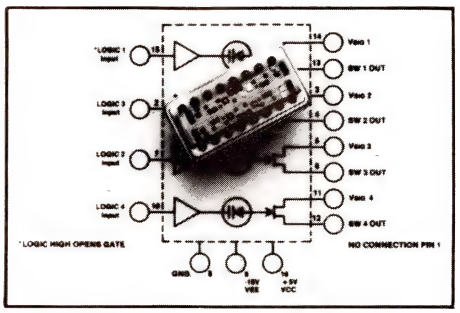
Gold-alloy inlaid contacts made the low-profile keyboard more reliable, the company says. In trifurcated contact design, three contact fingers ensure switch closure, even if foreign particles float into the contact area.

By incorporating integral jumpers into the switch contacts, the circuitry for a fully encoded keyboard fits on a single-sided pc board, for substantial savings over double-sided pc boards.

The Hi-Tek 725 measures 0.725 in. from the center of the home-row keycap to the bottom of the pc board. Key-switch travel is 0.140 in.; operating movement—stroke to make contact—is 0.070 in. The PC-122 sells for $85 each in volumes of 10,000. *–Ellie Aguilar*

Hi-Tek Corp., 7274 Lampson Ave., Garden Grove, Calif. 92641.
Phone (714) 898-9511 [Circle 408]

Ultra High Speed Quad Analog Gate



The CAG-49 features a turn-on time of 13 nanoseconds (typical), 5 times faster than monolithic analog switches in the same packaging space, and low ON resistance, typically 35 ohms, which remains constant with voltage. The CAG-49 is cost effective, selling for half the price of four switches purchased independently. The space advantage cuts costs in handling, stock and inventory. It's ideal for high speed store and hold and analog gating applications. Send for our free catalog.

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IMAGE RECORDER CUTS COST OF HIGH-QUALITY GRAPHICS

HP's $13,900 package translates color graphics from a personal computer into slides

A typical marketing manager for a mid-sized firm talked his employer into buying a personal computer because, among other things, he was impressed with its ability to produce high-quality graphics. As he grew fond of the machine, however, he also grew weary of its inability to share its diagrams and schematic artwork with a larger audience. What good are the graphics, he began to wonder, if he couldn't show them to anyone without dragging along the computer?

Getting presentation-quality graphics out of a computer and onto a 35-mm slide for projection during a sales meeting is neither simple nor cheap. Single slides can cost up to $50 and more, and it can take as many as three or four days for an outside lab to produce them. Moreover, film recorders—machines that take a computer-generated image from a CRT display and transpose it directly onto film—either rely on raster processing and lack high resolution or use expensive vector-recording methods.

Enter Hewlett-Packard with the HP 7510, an affordable color-film recorder. Based on the same vector-recording technology that is used in some dedicated graphics-reproduction systems, the stand-alone peripheral produces high-resolution slides from an image generated on virtually any personal computer.

Vector recording in itself is not new—it's been around for a while. What is new is that the technology—heretofore available only in systems costing up to $100,000 and more—has not previously been offered in the 7510's price range. HP is offering the 7510 in a $13,900 package.

Challenging companies such as Matrix Instruments, Polaroid, and Image Resource, all of which are well entrenched in raster-based film recording, HP also hopes its comparatively compact machine will use its high resolution (16,344 by 10,048 addressable points per frame) to compete with high-end vector machines as well.

The machine, which is about twice the size of the average personal computer, has its own high-resolution CRT that projects an image onto a standard roll of 35-mm film.

Prints, too. The screen in turn is photographed by a built-in 35-mm camera or by an optional Polaroid module that produces Polaroid SX-70 instant color prints measuring 3½ by 4½ in. Using this vector-recording method, the machine can reproduce a computer-generated image in 1 to 4 min.

HP is no stranger to the technology involved. "We build our own CRTs," says Nancy Ritzenthaler, product manager for the 7510 at HP. "We use the same ones as are used in our oscilloscopes, and we've got 20 years' experience there. Then we looked at the plotter, and we took those two products and kind of melded them together." HP is billing the 7510 as a companion to its eight-pen, high-end model 7550 plotter.

Users experienced with HP's HP-GL graphics language and the company's 7550 plotter will find that the plotter and the recorder are virtually interchangeable. Although the company will not elaborate, HP expects several of the more than 100 companies that make software drivers and support programs for the 7550 to introduce software support for the 7510 next week at Siggraph in San Francisco.

Vector recording has a number of advantages over its raster equivalent, not the least of which are its smaller appetite for computer memory and its faster processing speed. Because of the higher speeds, images can be recorded on film a full frame at a time; raster recorders create a line dot-by-dot and expose the film line by line.

To the office manager with one or two personal computers on his floor, the 7510's price may still seem a little steep. That is, HP points out, until he sits down and figures out that it costs more than $14,000 to have an outside company produce a dozen 30-slide presentations at $39 per slide.

Because one person or department within a company may not have that extensive a need for such a machine, HP has designed it so that it may be networked and used as a shared resource, thus optimizing its potential savings.

In addition, because an image described in vectors is condensed and can thus be sent efficiently over an interface, the 7510 uses an

Toastmaster. With Hewlett-Packard's recorder, 35-mm slides cost 25¢ each to make compared with the $39 for each slide that a service bureau would charge.

RS-232-C serial interface for all its I/O functions. An HP-IB interface is also included with the system, which will be sold on an original-equipment-manufacturer basis. *–Tobias S. Naegele*

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Rd., Palo Alto, Calif. 94303. [Circle reader service number 338]

POWER TRANSISTOR RESISTS LATCHUP

A second-generation insulated-gate transistor, the IGT4E10, has a 10-A 500-V rating at 100°C. Under a worst-case condition—150°C junction temperature—it handles peak latching currents at 30 A. Comparable devices with 10-A ratings have typical maximum latching current capabilities of less than 12 or 13 A at this junction temperature, the manufacturer says. The IGT4E10 is suitable for applications in which device junction temperatures frequently exceed 100°C.

One of the IGT family can replace Darlingtons with equivalent ratings. These transistors can also replace MOS FETs with similar current and voltage ratings in applications that operate at 20 kHz or below.

The IGT4E10 (500 V) and IGT4D10 (400 V) are rated at 2½ V (collector-emitter dc-saturation voltage) and have an equivalent static drain-source on-state resistance of 0.27 Ω. They are available now, in TO-220 packages, for $10 each in lots of 1,000. Devices in TO-3 packages are also available at similar ratings.

General Electric Co., Semiconductor Business Division, Building 7, Electronics Park, Syracuse, N.Y. 13221 [Circle 383]

DUAL GENERATOR PROGRAMS BAUD RATE

The MT1135 series of programmable dual baud-rate generators offers on-board master reference clocks. With four address lines and a strobe for each channel, the units permit independent selection of baud rates from 50 to 19,200 baud for each channel. They directly interface to microprocessor buses.

Master-clock frequency for the MT1135A and -B is 5.0688 Hz; for the MT1135C, 4.9152 MHz.

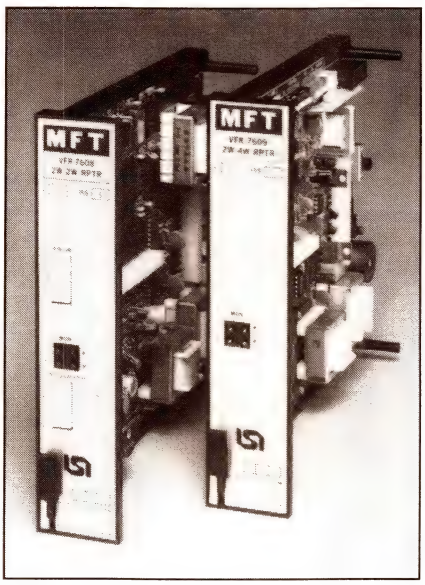
Available now, the MT1135 modules provide two baud-rate generators in a single 18-pin, hermetically sealed DIP. Final inspections include fine-leak tests according to MIL-STD-105 unless otherwise specified by the customer. In quantities of 5,000 to 10,000, the modules are priced at $8.90 each.

M-tron Industries Inc., P.O. Box 630, Yankton, S.D. 57078.
Phone (800) 762-8800 [Circle 381]

REPEATERS HANDLE SPECIAL CIRCUITS

Designed for use in standard Bell metallic-facilities-terminal bays or shelves, the model VFR-7609 family of voice-frequency repeaters (amplifiers) handle two-wire or four-wire special-service telephone circuits. Digital signal processing in real time allows these units to provide automatic balancing to line impedances, thus reducing setup and alignment procedures.

Unlike analog repeaters, the manufacturer says, these digital units are not subject to the drift problems associated with temperature changes or component



aging. Possible applications include terminal or intermediate use with loaded or nonloaded cable.

The single-quantity price of the VFR-7609 is $240; a two-wire-to-two-wire model, the VFR-7608, is $195. Both are available now.

Lear Siegler Inc., Electronic Instrumentation Division, 714 N. Brookhurst St., Anaheim, Calif. 92803.
Phone (714) 774-1010 [Circle 382]

GRAPHIC ICs HAVE HIGH RESOLUTION

A family of three ICs for graphics applications eases the design of graphics systems with resolutions better than 1,024 by 1,024 pixels.

The family consists of the AM8150 display-refresh controller, the AM8151 graphics color palette, and the AM8157 video shift register. The trio, all organized around a bit map, does not restrict designers to specific graphics processors, image-update techniques, or video standards, the company says.

The AM8151 reduces bit-mapped memory use and increases the number of colors available. It contains a 256-by-8-bit look-up table in fast ECL RAM and an 8-bit digital-to-analog converter. In quantities of 100 packaged in 40-pin ceramic DIPs, the part sells for $84.50 each.

The AM8150 addresses the bit map, refreshes the CRT and the dynamic RAM that compose the bit map, and supports pan and scroll functions. It comes in a 48-pin ceramic DIP and sells for $46 each in lots of 100. The AM8157 is a 20-bit parallel-to-serial video latch and shift register on a single chip. The 125-MHz part comes in a 40-pin ceramic DIP and sells for $37.50 each in 100-unit orders.

Advanced Micro Devices Inc., P.O. Box 3453, Sunnyvale, Calif. 94088.
Phone (408) 732-2400 [Circle 363]

IC STORES COLORS FOR GRAPHICS

Designed for implementation in color display systems, the IMSG170 integrates the functions of a color-mapping table, digital-to-analog converters, 75-Ω drivers, and an 8-bit microprocessor interface on a single CMOS chip.

The color-palette chip allows a pixel byte to be assigned one of 256 colors from a palette of 262,144 possible colors. The microprocessor interface provides direct modification of the 256-by-18-word color-table array, which is synchronized to the video data path.

Pricing and delivery information were not available at press time.

Inmos Corp., P.O. Box 16000, Colorado Springs, Colo. 80935. Phone (303) 630-4000 [Circle 361]

CHIP CODES, DECODES FOR NETWORKS

Operating at data rates up to 2 Mb/s, the SL3000 Manchester encoder/decoder is a silicon-gate CMOS IC that connects local-area-network controllers and transceivers.

The device encodes nonreturn-to-zero transmit data into Manchester format and decodes Manchester-encoded receive data into NRZ format. The chip's digital phase-locked-loop circuit extracts and synchronizes the receive clock to the receive data. Other features include detection of data-transmission collisions and Manchester-encoding format violations as well as local loopback capability.

In quantities under 100, the part sells for $49 each. Delivery takes about 12 weeks. Samples are available now in 20-pin plastic DIPs. Production quantities will be ready in September.

Universal Semiconductor, Inc., 1925 Zanker Rd., San Jose, Calif. 95112. Phone (408) 279-2830 [Circle 362]

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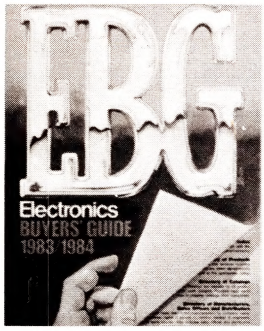

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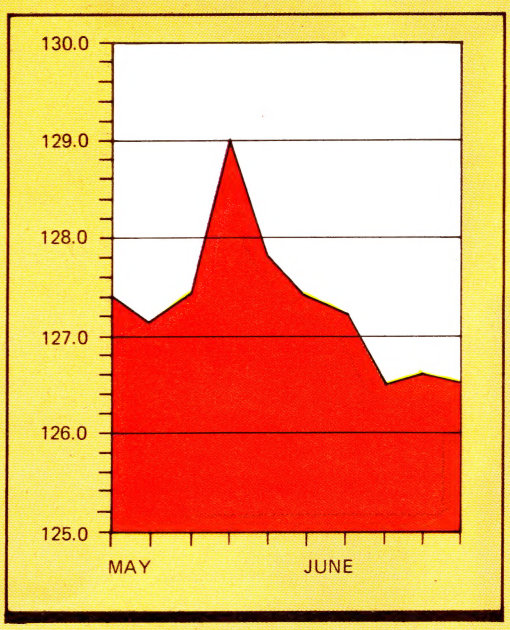
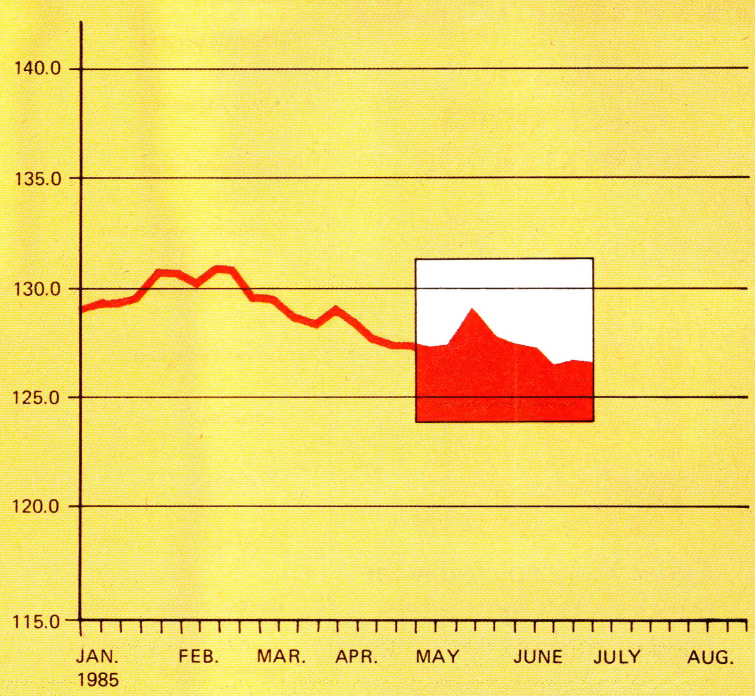
ELECTRONICS INDEX



THIS WEEK = 126.5
LAST WEEK = 126.6
YEAR AGO = 126.5
1982 = 100.0



The *Electronics* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

U.S. ELECTRONICS SHIPMENTS

Shipments ($ billions)	May 1985	April 1985	May 1984
Communications equipment	4.912	4.781	4.457
Radio and TV receiving equipment	0.893	0.941	0.932
Electronic and electrical instruments	4.772	4.699	4.534
Components	3.168	3.200	3.672

U.S. GENERAL ECONOMIC INDICATORS

	May 1985	April 1985	May 1984
Index of leading economic indicators	167.8	166.6	168.2
Budgeted outlays of the federal government ($ billions)	80.245	82.228	71.391
Budgeted outlays of the Department of Defense ($ billions)	22.198	20.239	19.955
Operating rate of all industries (% capacity)	78.3	78.4	79.7
Industrial-production index	165.3	165.5	162.8
Total housing starts (annual rate in thousands)	1,663	1,937	1,787

Hurt by slack shipments of electronics equipment, the *Electronics* Index slipped 0.1% in the latest week. Suffering the most damage were shipments of radio and TV equipment, which dropped 5% in May (the latest month for which data is available). Reflecting the industry's woes, shipments of components fell 1%.

On the plus side, shipments of instruments and communications equipment both rose in the month. Instruments shipments gained 1.5%; communications gear increased 3%. The index of leading indicators was up 0.8% in the month, an encouraging performance given the economy's relatively slow growth in the first quarter. Despite an unexpected tumble in housing starts in May, this sector should benefit in the coming months from recent declines in mortgage rates.

Overall, with the prime interest rate inching downward, business investment should keep the general economy afloat for a while longer. The longer the economy as a whole stays healthy, the better the chances are that the electronics industry will climb out of the doldrums.

A PLACE
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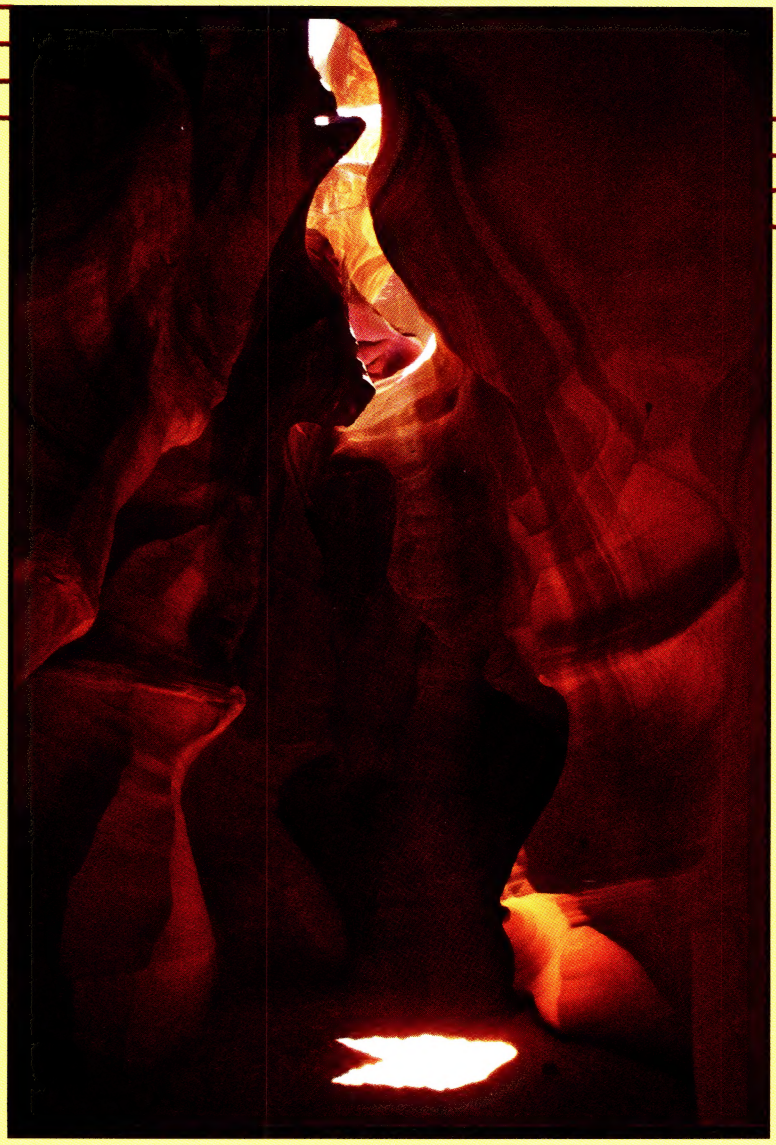

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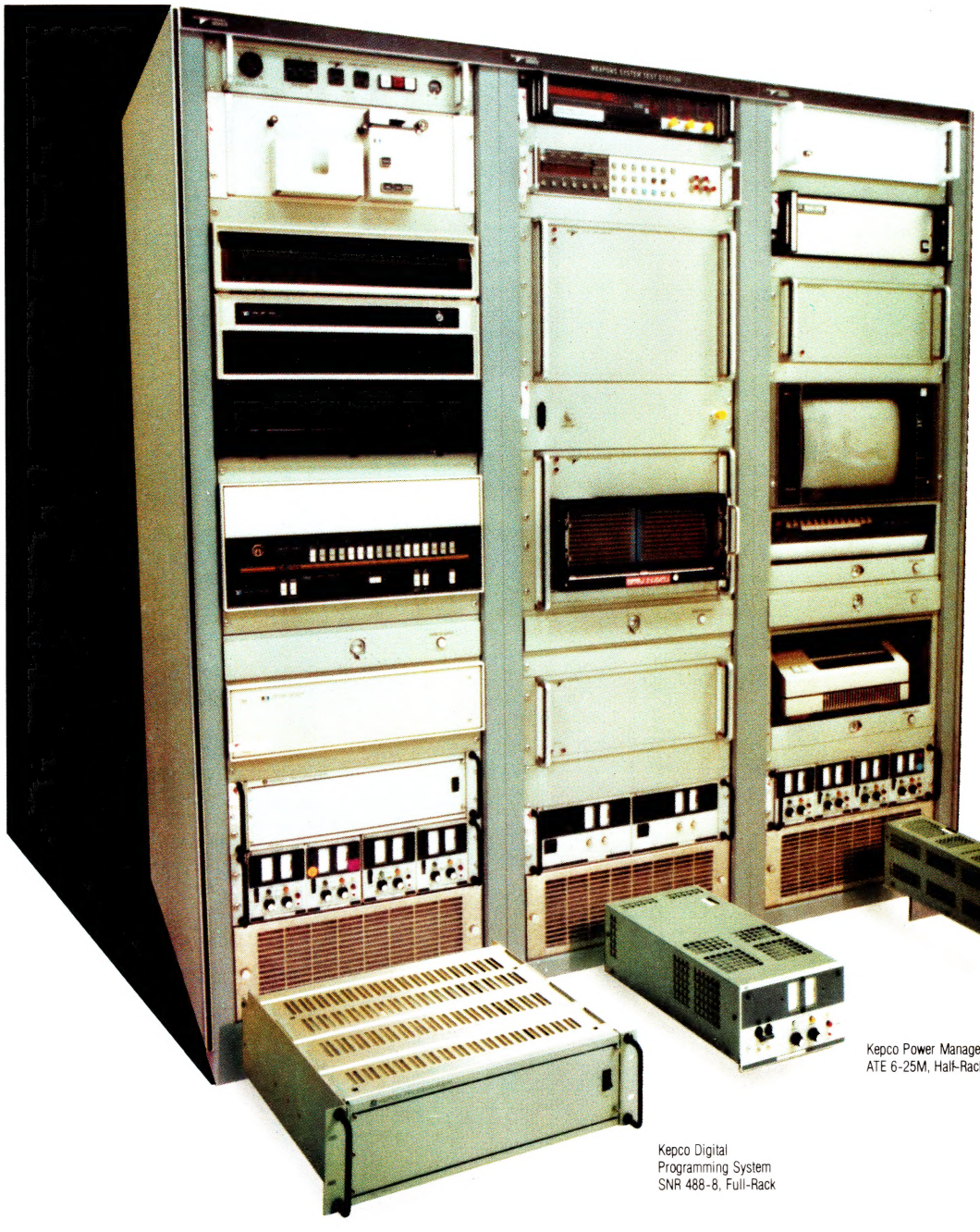

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